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An Investigation of Border Traps and Interface States in High- k /InGaAs Metal- Oxide-Semiconductor Systems

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Abstract

The innovation and scaling of complementary metal oxide semiconductor field effect transistor (CMOS) at the heart of integrated circuits has been on-going for the last four decades. The materials themselves now become the limit to further reduction of device dimensions. For instance, the scaling of the conventional Si/SiO₂ metal-oxide-semiconductor field effect transistor (MOSFET) has come to its limit as the ultra-thin SiO₂ layer introduces unacceptably large leakage current via electron direct tunnelling. Thus incorporation of new materials into semiconductor processes is needed for devices with smaller dimensions and higher performance. High mobility materials (e.g. In_{0.53}Ga_{0.47}As) and high dielectric constant (high-*k*) gate materials are potential candidates being researched to replace Si/SiO₂ structure to achieve lower leakage, lower power dissipation and higher speed of device operation.

In order to realize high performance high-*k*/In_{0.53}Ga_{0.47}As MOS devices, there are a few problems that must be resolved, one of which is the high density of electrically active defects that exist near/at the high-*k*/In_{0.53}Ga_{0.47}As interface, which can induce device instability. In this thesis, investigation into border traps (or charge trapping) and interface states in HfO₂/In_{0.53}Ga_{0.47}As and Al₂O₃/In_{0.53}Ga_{0.47}As MOS capacitor structures was carried out with an emphasis on the characterization of border traps using capacitance-voltage (C-V) hysteresis measurement.

The charge trapping behavior is observed to be predominantly a reversible process and the density of trapped charge (Q_{trapped}) estimated from C-V hysteresis can be comparable to, or even greater than the typical high-*k*/In_{0.53}Ga_{0.47}As interface state density, highlighting that the C-V hysteresis is a serious problem to resolve. It is observed that MOS systems with removed high-*k*/In_{0.53}Ga_{0.47}As interface layer exhibit a significant reduction in C-V hysteresis and charge trapping when compared to samples which have an interface layer between high-*k* oxide and In_{0.53}Ga_{0.47}As. Moreover, based on an oxide thickness series for both HfO₂ and Al₂O₃, it is demonstrated that the

C-V hysteresis increases linearly with the increasing high- k oxide thickness and the corresponding Q_{trapped} is a constant value over all the oxide thicknesses. These experimental observations indicate that the trapped charge is predominately localized as a sheet charge (in cm^{-2}) near/at the interfacial transition region between the high- k oxide and the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ substrate, which can contain native oxides of In, Ga and As. The engineering of the high- k / $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface is therefore the key to reducing C-V hysteresis and improving device reliability. In this work, a systematic study of the effect of forming gas annealing (5% H_2 / 95% N_2) at a series of temperatures (250°C ~ 450°C for 30min) on the electrical characteristics of $\text{HfO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS systems was carried out, demonstrating the ability to reduce border trap density values with anneals in (5% H_2 / 95% N_2) for $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and $\text{HfO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS structures under certain conditions.

C-V hysteresis was also studied with a varying stress time in accumulation for high- k / $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS system. It is observed that C-V hysteresis increases with a power law dependence with the increasing stress time at the initial stage of stressing and tends to reach a plateau at sufficiently long stress times due to the filling of almost all the pre-existing charge trapping states. It is also demonstrated for high- k / $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS system that a significant portion of trapped charge can be removed from the trapping sites within $\sim 4\text{s}$ after the stress voltage is removed.

Finally, a combined C-V and hard x-ray photoelectron spectroscopy (HAXPES) study was performed on $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors using both high (Ni) and low (Al) work function metal gates. The HAXPES analysis reveals the presence of band bending prior to metal deposition due to a combination of fixed oxide charges and possible donor-type interface states. The Fermi level movement following metal deposition reveals a partially pinned $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface. The Fermi level position at zero gate bias was calculated using both C-V and HAXPES analysis, and a reasonable agreement was achieved between the two techniques. This combined study thus provides more certainty on the interface state profile

($D_{it}(E)$) extractions and also helps to bridge the gap between interface chemistry and electrical properties at a buried interface.

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Saving the most important comment to last, I wish to convey my sincerest appreciation to my mother, Yiman, for her love, support and encouragement throughout my life. Without her support, I would never have had the opportunity to travel to Ireland to study. This thesis is dedicated to her.

Declaration

I, Jun Lin, certify that this thesis is my own work and I have not obtained a degree in University College Cork or elsewhere on the basis of the work submitted in this thesis.

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List of symbols

C_m	Measured capacitance of MOS capacitor [F/m ²]
C_{\max}	Maximum capacitance of MOS capacitor in nominal accumulation [F/m ²]
C_{\min}	Minimum capacitance of MOS capacitor [F/m ²]
C_s	Semiconductor differential capacitance [F/m ²]
C_{total}	Total capacitance of MOS capacitor [F/m ²]
C_{fb}	Capacitance at flatband condition [F/m ²]
C_{it}	Capacitance associated with interface states [F/m ²]
C_{ox}	Oxide capacitance [F/m ²]
C_{IL}	Capacitance of any interfacial layer formed in MOS capacitor [F/m ²]
C_{HF}	High-frequency capacitance [F/m ²]
C_{LF}	Low-frequency capacitance [F/m ²]
D_{it}	Interface state density [cm ⁻² eV ⁻¹]
ΔE_c	Conduction band offset between oxide and semiconductor [eV]
ΔE_v	Valence band offset between oxide and semiconductor [eV]
ΔV	C-V hysteresis of MOS capacitor (with/without stress time) [V]
ΔV_0	C-V hysteresis of MOS capacitor (without stress time) [V]
ΔV_T	Threshold voltage shift in MOSFET [V]
E_c	Conduction band minimum Energy [eV]
E_F	Fermi level energy [eV]
E_i	Intrinsic Fermi level energy of the semiconductor[eV]
E_g	Semiconductor bandgap energy [eV]
E_{ox}	Electric field across the oxide (or oxide field) [MV/cm]
E_v	Valence band maximum energy [eV]
ϵ_0	Permittivity of free space [F/m]
ϵ_s	Dielectric constant of semiconductor

Φ_B	Bulk potential of MOS capacitor [V]
Φ_{ms}	Work function difference between metal and semiconductor [eV]
ϕ_b	Barrier height [eV]
G	Conductance of MOS capacitor [S/m^2]
G_m	Measured conductance [S/m^2]
G_p	Parallel conductance [S/m^2]
h	Planck's constant
$\eta_{trapping}$	Charge trapping efficiency
I_d	Drain current of MOSFET [A]
J_{DT}	Leakage current caused by direct tunnelling [A/cm^2]
J_{FN}	Leakage current caused by Fowler-Nordheim tunnelling [A/cm^2]
k	Dielectric constant or relative permittivity
k_B	Boltzman's constant [J/K or eV/K]
λ	Sampling depth of HAXPES measurements [nm]
λ_D	Debye length [nm]
L	Gate length of MOSFET [m]
m	Free electron mass [kg]
m_{ox}	Effective electron mass in the oxide [kg]
n_i	Intrinsic concentration of semiconductor [cm^{-3}]
n_s	Electron density at semiconductor surface [cm^{-3}]
N_c	Effective density of states in conduction band [cm^{-3}]
N_a	Doping concentration of p -type semiconductor substrate [cm^{-3}]

N_d	Doping concentration of n -type semiconductor substrate [cm^{-3}]
N_{doping}	Doping concentration of semiconductor substrate [cm^{-3}]
N_v	Effective density of states in valence band [cm^{-3}]
p_s	Hole density at semiconductor surface [cm^{-3}]
q	Elementary charge [C]
Q_f	Fixed oxide charge [C/cm^2 or C/cm^3]
Q_{it}	Charge associated with interface states [C/cm^2]
Q_{injected}	Injected charge density [cm^{-2}]
Q_{ot}	Trapped charge in the oxide [cm^{-2}]
Q_s	Surface charge density of MOS capacitor [cm^{-2}]
Q_{trapped}	Trapped charge density at/near oxide/semiconductor interface [cm^{-2}]
t_{relax}	Relaxation time [s]
t_{stress}	Stress time (or hold time) in accumulation [s]
t_{ox}	Oxide thickness [m]
T	Temperature [K]
μ	Effective mobility of channel carrier [cm^2/Vs]
V_d	Drain voltage of MOSFET [V]
V_{fb}	Flatband voltage [V]
V_g	Gate voltage applied to MOS capacitor or MOSFET [V]
V_{max}	Maximum voltage applied to MOS capacitor in nominal accumulation [V]
V_{ov}	Overdrive voltage [V]
V_{ox}	Voltage drop across oxide [V]
V_T	Threshold voltage of MOSFET [V]
ω	Angular frequency [rad/s]
w	Depletion layer width [nm]

w_{\max}	Maximum depletion layer width [nm]
W	Gate width of MOSFET [m]
Ψ	Potential at any point in semiconductor of a MOS capacitor [V]
Ψ_s	Surface potential of MOS capacitor [V]

List of Acronyms

ac	alternating current
ALD	Atomic Layer Deposition
BE	Binding Energy
CMOS	Complementary Metal-Oxide-Semiconductor
C-V	Capacitance-Voltage
CVD	Chemical Vapor Deposition
DC	Direct Current
EPR	Electron Paramagnetic Resonance
FGA	Forming Gas Annealing
FWHM	Full Width Half Maximum
G-V	Conductance-Voltage
HAXPES	Hard X-ray Photoelectron Spectroscopy
HR-TEM	High Resolution Transmission Electron Microscopy
I-V	Gate Current-Voltage
J-V	Gate Current Density-Voltage
MOS	Metal-Oxide-Semiconductor
MOSCAP	Metal-Oxide-Semiconductor Capacitor
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
MOVPE	Metal Organic Vapor Phase Epitaxy
RTA	Rapid Thermal Annealing

TEM	Transmission Electron Microscopy
TEMAH	$\text{Hf}[\text{N}(\text{CH}_3)\text{C}_2\text{H}_5]_4$
TMA	Trimethyl-Aluminum $[\text{Al}(\text{CH}_3)_3]$
XPS	X-ray Photoelectron Spectroscopy

Chapter 1: Introduction

1.1 Introduction

The objective of this chapter is to place the research work of the thesis in the general context of complementary metal-oxide-semiconductor (CMOS) technology and the challenges associated with the future scaling of minimum metal-oxide-semiconductor field effect transistor (MOSFET) dimensions. The sections 1.2-1.4 introduce the background to the thesis and in particular the motivation behind using high- k /III-V channel materials for future devices. The challenges in developing high performance high- k /III-V MOS devices will be emphasized in section 1.5, highlighting open questions which form the basis of the research work in the thesis. Section 1.6 outlines the overall structure of the thesis.

1.2 MOSFET Scaling

Metal-oxide-semiconductor field effect transistors (MOSFETs) are the fundamental switching elements of integrated circuits. The innovation and scaling of MOSFET dimensions have been on-going for the last four decades. The scaling of MOSFET dimensions has allowed for increased functionality per chip area, improved logic characteristics and reduced price per chip. The structure of a traditional n -channel MOSFET structure is illustrated in Figure 1.1, where L and W are the MOSFET gate length and width, respectively. The gate length dimensions of SiO_2/Si based MOSFETs was scaled from values around $10\mu\text{m}$ in the early 1970's down to values around 65nm in 2007 following the Moore's law (Figure 1.2), which was

brought up by Gordon Moore in 1965, who predicted that the density of transistors on a single chip doubles every 18 months [1]. The reason for the use of the SiO_2 as the gate insulating layer in MOSFETs is due to the excellent insulating property of SiO_2 and the very low values of oxide charge and interface states (typically $\leq 10^{10} \text{cm}^{-2}$) which can be achieved in the SiO_2/Si system which forms the active region of the metal-oxide-semiconductor (MOS) structure. Until recently, polysilicon was typically used as the “metal” gate for SiO_2/Si based MOSFET due to its ability to form self-aligned gates and the fact that the work function difference between polysilicon and the channel material (i.e. Si) can be engineered to be close to zero in inversion based on doping of the polysilicon gate, which decreases the threshold voltage. This allows more control of the threshold voltage when compared to using a single metal as the gate electrode (e.g. aluminum).

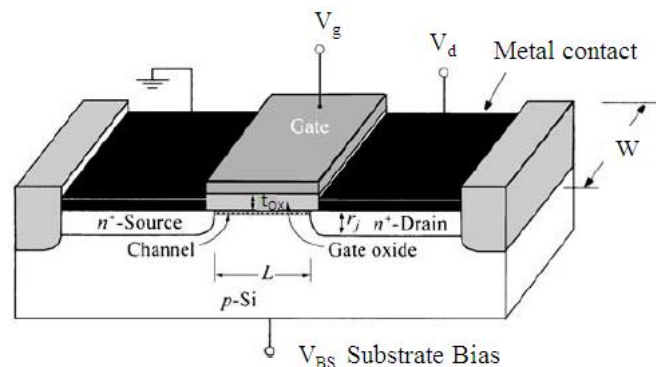


Figure 1.1: Structure of an n-channel MOSFET [2].

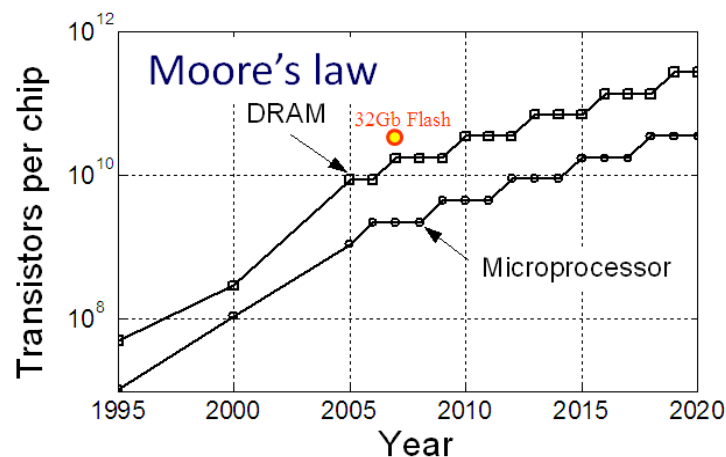


Figure 1.2: Moore's Law.

In the MOSFET performance, a high drive current (or I_d , see equation (1.1)) is required.

$$I_d = \mu W C_{ox} (V_g - V_T - \frac{1}{2} V_d) \frac{V_d}{L} \quad (1.1)$$

where μ is the channel carrier mobility, V_g is the voltage applied to the gate, V_T is the threshold voltage, V_d is the voltage applied to the drain region and C_{ox} is the oxide capacitance defined by equation (1.2).

$$C_{ox} = \frac{\epsilon_0 k}{t_{ox}} \quad (1.2)$$

where ϵ_0 is the vacuum permittivity (8.85×10^{-12} F/m), k is relative permittivity of the oxide and t_{ox} is the thickness of the oxide.

The scaling of oxide thickness is needed in order to increase the oxide capacitance, thus allowing a smaller voltage to form the same amount of charge in the channel and induce the same or even increased drive current. However, the scaling of the SiO_2 has effectively come to its limit as any further reductions in the ultra-thin SiO_2 layer, which was approaching a thickness value of just a few atomic layers, will result in unacceptably large leakage currents via direct electron tunnelling, leading to a very large power dissipation and reduced device reliability [3]. This demands for the research into new materials which can provide both increased oxide capacitance and low gate leakage in the gate stack to replace SiO_2 . Therefore, high dielectric constant (high- k) materials are introduced as the solution to resolve the gate leakage issue.

1.3 High- k /Metal Gate Stack

The dielectric constant of SiO_2 is 3.9. Any materials used in MOS devices to replace SiO_2 and have a higher dielectric constant than 3.9 can be referred to as high- k materials. A high value of oxide capacitance is required in MOSFET performance in order to assure a high drive current. From equation (1.2), either increasing the k -value or reducing the oxide thickness can increase the oxide capacitance. With the introduction of high- k gate materials to MOS devices, the physical thickness of the oxide can be increased while maintaining or even increasing the oxide capacitance, thus efficiently

reducing the gate leakage current and the overall power dissipation while ensuring a high drive current. There are some important requirements and issues when high- k materials are considered as a replacement of SiO₂ on Si based MOSFET listed below.

(1) For the high- k oxide to be a good insulator, it must possess a sufficient band offset with the semiconductor band edges to minimize the Schottky emission and direct tunnelling effect [4, 5]. A high- k on Si transistor review paper by John Robertson [4] has summarized the k -value of a selection of high- k candidates and their corresponding bandgap as well as the band offset with Si conduction band (CB) edge (see Table 1.1), showing that there is a trade-off between the k -value and the band offset. A compromise must be made when choosing the suitable high- k gate material.

Table 1.1 Static dielectric constant (k), experimental bandgap and (consensus) CB offset on Si of the candidate gate dielectrics (Source of Table 1.1: J. Robertson [4])

	K	Gap (eV)	CB offset (eV)
Si		1.1	
SiO ₂	3.9	9	3.2
Si ₃ N ₄	7	5.3	2.4
Al ₂ O ₃	9	8.8	2.8 (not ALD)
Ta ₂ O ₅	22	4.4	0.35
TiO ₂	80	3.5	0
SrTiO ₃	2000	3.2	0
ZrO ₂	25	5.8	1.5
HfO ₂	25	5.8	1.4
HfSiO ₄	11	6.5	1.8
La ₂ O ₃	30	6	2.3
Y ₂ O ₃	15	6	2.3
a-LaAlO ₃	30	5.6	1.8

(2) Unlike SiO₂, which is the Si native oxide and can be thermally grown on Si substrate, high- k oxides must be deposited. Atomic layer deposition (ALD) is one of the leading deposition methods for high- k oxides in which two or more precursors are introduced to a vacuum deposition chamber in a sequential manner. The first precursor being introduced carries the metal reactant needed for the high- k oxide (e.g. Al(CH₃)₃ (TMA) for the deposition

of Al_2O_3 and $\text{Hf}[\text{N}(\text{CH}_3)\text{C}_2\text{H}_5]_4$ (TEMAH) for the deposition of HfO_2) and the second precursor is oxidant (e.g. H_2O vapor). After each precursor pulse, saturation in chemisorption on the film growing surface can be achieved, followed by a purge phase which pumps away the excess precursors and any reaction by-products. These terminate the reaction to one atomic layer after each precursor pulse phase and complete an ALD cycle, allowing excellent uniformity of ALD. The ALD cycle is then repeated in order to grow the targeting oxide thickness. Figure 1.3 shows schematically a complete cycle of ALD of Al_2O_3 using TMA and H_2O as precursors [6]. Due to the ability to grow controllable thin films, as the thickness can just be determined simply by the number of ALD cycles, ALD is preferably adopted as the high- k oxide deposition method for research purposes. Other deposition methods include chemical vapor deposition (CVD) (also preferred in industry), electron beam evaporation plus oxidation and sputter oxidation. A comparison of the mentioned deposition methods in terms of coverage, purity, defects, etc is given by [4].

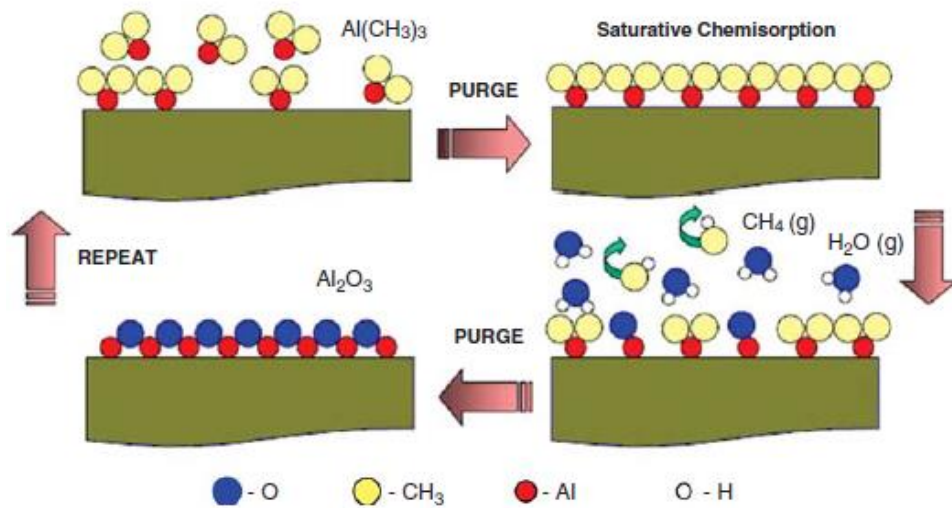


Figure 1.3: A complete ALD cycle in the deposition of Al_2O_3 using TMA and H_2O as precursors, from the review of R. M. Wallace et al [6].

(3) As high- k materials are introduced to replace SiO_2 in MOSFET, polysilicon is no longer suitable to be the gate material because polysilicon reacts with the high- k oxide, adding an unwanted capacitance to the gate stack and causing Fermi level pinning at the high- k /polysilicon interface thus

giving rise to a very high threshold voltage and reduced drive current. Metal gates are thus chosen to replace polysilicon gate to prevent the reaction with high- k dielectric. In addition to the incompatibility between high- k oxide and polysilicon, phonon scattering in high- k oxide is a problematic issue that causes mobility degradation. Metal gates have been reported to effectively screen the phonon scattering from coupling with the channel carriers and resolve the mobility degradation [7]. However, challenge in using metal gate remains as the chosen metal has to have a suitable work function for both n -MOS and p -MOS to achieve high performance. In late 2007, INTEL introduced a HfO_2 based high- k material and metal gate into the gate stack of 45nm MOSFETs (see Figure 1.4) [8]. This is a significant innovation in the development of CMOS technology and the first time high- k /metal gate stack was put into commercial manufacturing process.

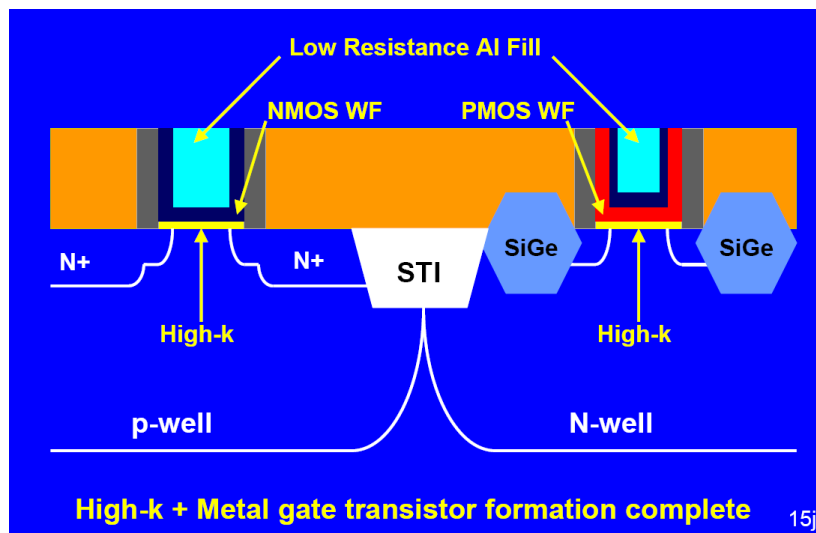


Figure 1.4: High- k /metal gate into the gate stack of 45nm MOSFETs (Source: K. Misty et al., IEDM 2007).

(4) In high- k /Si MOS structures, a thin SiO_2 layer is formed between high- k layer and Si substrate. The SiO_2 interfacial layer, which has a low k -value and introduces an extra capacitance in series with the high- k oxide capacitance, reduces the overall capacitance of the gate stack. However, this interfacial SiO_2 layer is needed as experiments have shown that when the high- k oxide is in direct contact with the silicon channel, the carrier mobility

in the channel region is reduced thus slowing the switching speed of MOSFETs [9, 10].

One potential solution to further enhance MOSFET performance is to replace Si channel with high mobility channel materials, such as III-V materials for the *n*-channel device and Ge for the *p*-channel device, and to integrate the alternative channel materials with high-*k* oxides, which is discussed further in section 1.4.

1.4 High Mobility Channel Materials

III-V compound semiconductors, comprising elements from group III and group V of the periodic table, are being explored as new channel materials for MOS devices. The main reason for III-V to be used to replace Si is that III-V materials have very high electron mobility. For instance, GaAs has an electron mobility of $8500\text{cm}^2/\text{Vs}$ and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ has an even higher electron mobility of $14000\text{cm}^2/\text{Vs}$ compared to $1400\text{cm}^2/\text{Vs}$ for Si (see Table 1.2).

Table 1.2 Comparison of carrier mobility

Material	Si	Ge	GaAs	$\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$	InAs	InSb
Electron Mobility (cm^2/Vs)	1400	3900	8500	14000	40000	78000
Hole Mobility (cm^2/Vs)	450	1900	400	300	500	850

By employing such high mobility materials in MOSFETs, the drive current can be increased (see equation (1.1)) and thus a higher speed of switching can be achieved. Due to the high electron mobility III-V materials possess, III-V materials are commonly used as the channel materials for *n*-channel MOSFETs. It is notable from Table 1.2 that the hole mobility of both Si and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ are small, therefore high hole mobility materials such as Ge are now considered as a channel material option for *p*-channel MOSFET. An

alternative way to utilize the high mobility materials is to use the higher mobility to achieve the same drive current at a lower supply voltage, which has the potential to reduce overall power consumption in the device. The combination of III-V *n*-MOS and Ge *p*-MOS transistors using high-*k* oxides for the future CMOS technology is expected to improve the performance over power consumption ratio. Due to the combination of a high electron mobility, suitable energy gap (0.75eV) and the fact that it can be grown lattice matched in InP for initial investigations, there has been a considerable focus of research attention on $\text{In}_x\text{Ga}_{1-x}\text{As}$ with a 53% indium concentration (referred to as $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$). This thesis focuses on the study of MOS system formed on $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ grown by metal organic vapour phase epitaxy (MOVPE) on InP substrates.

1.5 Challenges in Developing High Performance High-*k*/III-V MOS Devices

From the discussions in session 1.3 and 1.4, high-*k* oxides in conjunction use with III-V channel materials in MOSFET has the potential for lower leakage, lower power consumption and higher speed of device operation. However, there are a number of challenges associated with the incorporation of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ channel materials into a CMOS process, which include:

- Integration of the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ channel onto a silicon platform by growth or bonding.
- Integrating a high hole mobility channel with the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ *n*-channel MOSFET for the complementary *p*-channel device.
- Minimizing resistance in the source and drain contacts.
- Electrically active defects present in the high-*k*/III-V gate stack.

This thesis is focused on the issue of the high-*k*/III-V gate stack, which typically is reported to have a high density of electrically active defects both at the interface and in the oxide layer which can degrade the electrical characteristic of MOSFETs and induce device instability. The main electrically active defects include fixed oxide charges within the high-*k* oxide, high-*k*/III-V interface states, and border traps as illustrated in Figure

1.5. A realistic target of the density of these defects for device applications in practice is $\leq 1 \times 10^{11} \text{cm}^{-2}$. Understanding the origin of these defects, finding practical routes to the passivation of these defects and realizing high performance high- k /III-V MOS devices, which are the objective of this work, are very important in developing future III-V devices for integrated circuits. For research purposes, metal-oxide-semiconductor (MOS) capacitors are often used to study these defects instead of fabricating a full MOSFET, as it reduces the associated processing steps and cost. The work in this thesis is focused on MOS structures and the theory behind the MOS structure and the corresponding capacitance-voltage response is covered in Chapter 2.

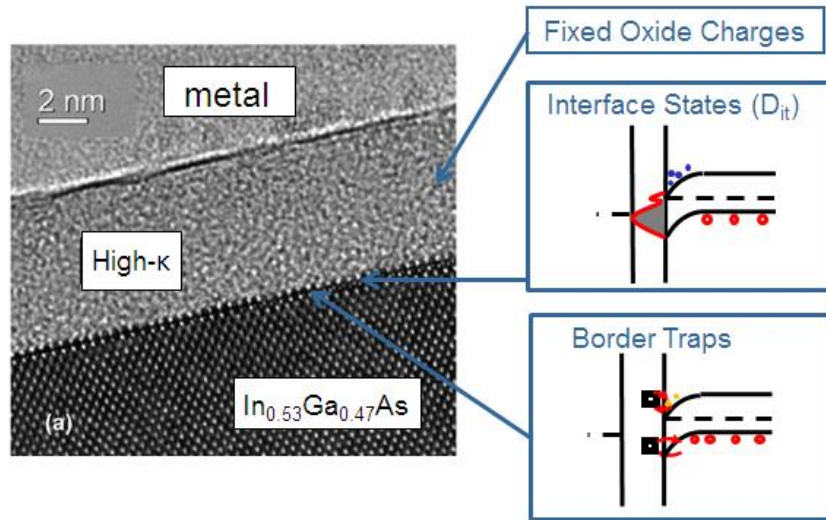


Figure 1.5: Illustration of electrically active defects in high- k /In_{0.53}Ga_{0.47}As MOS system.

The electrically active defects illustrated in Figure 1.5 are discussed separately as below.

(1) Fixed Oxide Charges

Fixed charges (Q_f) are immobile charges distributed within the oxide and do not respond to the gate voltage. Fixed oxide charges can cause the MOSFET threshold voltage to shift and the oxide charge can be either positive or negative depending on the specific oxide and annealing conditions. Fixed oxide charges can arise from oxidation/deposition process. It is suggested in [2] that for SiO₂, the fixed oxide charges origin from excess Si or the loss of

an electron from excess oxygen centres near the SiO₂/Si interface. Recent work demonstrated that fixed charge in the ALD deposited Al₂O₃ in Al₂O₃/In_{0.53}Ga_{0.47}As MOS systems is comprised of negative interface fixed charge near the Al₂O₃/In_{0.53}Ga_{0.47}As interface and positive fixed charge distributed through the bulk of Al₂O₃ film [11]. The origin of fixed charges in ALD deposited Al₂O₃ is suggested to be oxygen and aluminium dangling bonds and post-metal forming gas anneal (FGA, 5 % H₂/ 95% N₂) is reported to efficiently reduce the fixed oxide charge density as shown in Figure 1.6 [11, 12].

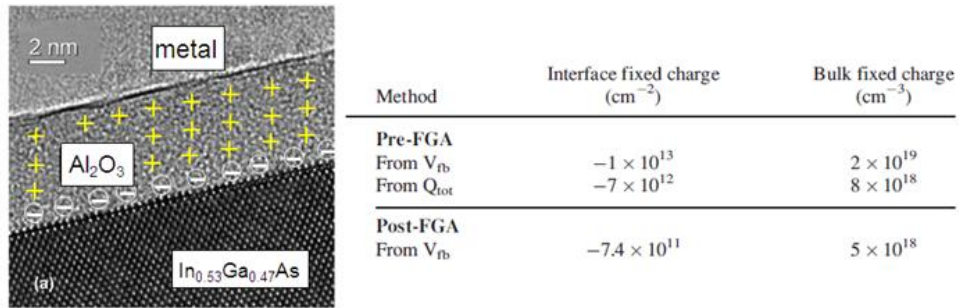


Figure 1.6: Fixed oxide charge in ALD-deposited Al₂O₃ is comprised of positive bulk fixed charge and negative interface fixed charge, both of which are reduced after FGA [11].

(2) Interface States

Interface states between the oxide and semiconductor in MOS devices can introduce extra energy levels within the semiconductor bandgap which restrict efficient Fermi level movement thus slowing down the device switching speed. For very high interface state density values (typically $> 1 \times 10^{13} \text{cm}^{-2}$), the interface state density is so high that the semiconductor surface Fermi level is pinned preventing the inversion channel from being formed.

The interface state density (D_{it}) for high- k /III-V MOS structures can be one or even two orders of magnitude higher than that of SiO₂/Si structures. The Si dangling bonds (known as P_{b0} and P_{b1} centers) are suggested to be the origin of the interface states for SiO₂/Si MOS systems [13-15]. However, the

interface between high- k oxide and III-V substrate can be very complicated. For example, high- k /In_{0.53}Ga_{0.47}As interface can contain In_{0.53}Ga_{0.47}As native oxides of In, Ga and As, which are presented in a variety of bonding configurations [16]. The physical origin of interface states can be dangling bonds, dimmers (e.g. As-As [17]) and anti-site defects (e.g. As_{Ga}) at that very interface. Figure 1.7 illustrates a typical interface state density profile (i.e. D_{it} as a function of the energy level E with respect to the valence band edge E_v) for an Al₂O₃/In_{0.53}Ga_{0.47}As structure, showing a donor-type D_{it} profile that increases towards the valence band edge with a peak D_{it} near the midgap and an acceptor-type D_{it} profile that increases into the conduction band [18]. An alternative way in which the native oxides can affect the device performance is that these oxides in direct contact with the In_{0.53}Ga_{0.47}As surface have a smaller energy gap (e.g. In₂O₃=3.75eV, Ga₂O₃=4.8eV [19]) than the high- k oxide thus leading to increased leakage. Moreover, an electron trapping well can be formed at the interface between the interfacial native oxide and the In_{0.53}Ga_{0.47}As substrate causing device instability. Therefore the research into the high- k /In_xGa_{1-x}As interface states is complex and has received considerable research attention in the literature [5, 11, 16-18, 20-24].

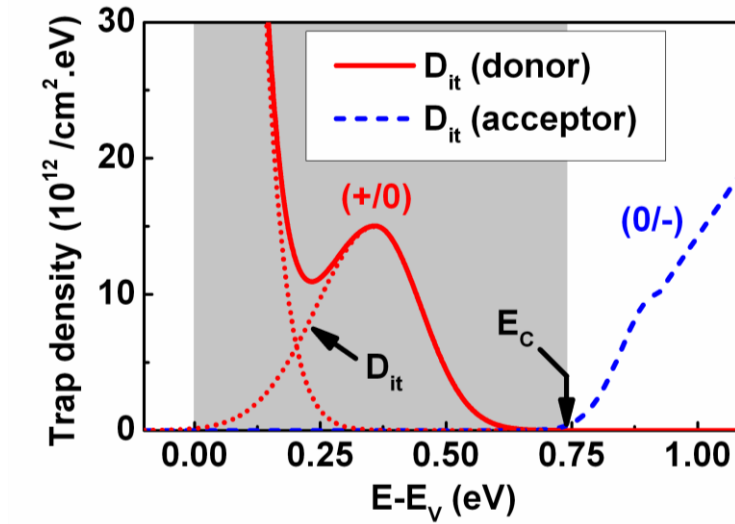


Figure 1.7: Typical interface state density profile in Al₂O₃/In_{0.53}Ga_{0.47}As MOS device. Source of Figure 1.7: V. Djara et al [18].

For the study of interface states, the primary task is to quantify the interface state as a function of energy level correctly. Electrical characterization such

as capacitance method and conductance method is universally used to quantify D_{it} [2, 25]. However, cautions must be taken when using these methods for the extraction of D_{it} for high- k /III-V MOS systems as they can only be valid under some limited conditions and the capacitance-voltage characteristics can be easily misinterpreted due to the confusion between interface state response and minority carrier response [26], leading to a large error in D_{it} . There is a variation of reported D_{it} values between different research groups using different D_{it} extraction methods [5]. The validity of the electrical methods and determination of accurate D_{it} will be further examined in this thesis.

A variety of passivation methods have been reported to reduce D_{it} level such as in-situ H_2S passivation [16, 20], forming gas anneal [11, 21, 27, 28] and annealing in N_2 [28]. Another approach is to use an interface Al_2O_3 control layer in $HfO_2/In_{0.53}Ga_{0.47}As$ MOS system, which is effective in D_{it} reduction attributed to the “self-cleaning” process of ALD of Al_2O_3 on $In_{0.53}Ga_{0.47}As$ surface [29-31]. Recent work on high- $k/In_{0.53}Ga_{0.47}As$ MOS systems has shown that $(NH_4)_2S$ (10% in deionized H_2O) for 20min at room temperature prior to the ALD with a minimum transfer time from the aqueous $(NH_4)_2S$ solution to the ALD chamber is effective in suppressing the formation of $In_{0.53}Ga_{0.47}As$ native oxide and reducing D_{it} [32]. This surface passivation method is used for the majority of the $In_{0.53}Ga_{0.47}As$ samples presented in this thesis.

(3) Border Traps

Border traps (also referred to as “charge trapping states” or “slow traps” to distinguish from the interface states which have very fast response times) were firstly studied by D. M. Fleetwood *et al* [33] back in 1995. Border traps describe those defects with energy levels aligned with the MOS semiconductor conduction/valence bands and can exchange charges with the bands via a tunnelling process and have been examined in the literature [34-38]. The charge exchange following an ac signal of different frequencies superposed on the gate voltage will result in a dispersion in the capacitance value with the ac frequency for MOS capacitors biased in accumulation (This

effect is often called frequency dispersion and is covered in chapter 2). This effect is similar to the way in which interface states will impact the capacitance-voltage response and as a consequence there has been confusion between border traps and interface states. A potential way to distinguish interface states from border traps is to analyze the MOS accumulation frequency dispersion with varying measurement temperature, as the interface states are temperature dependent but the direct tunnelling process depends only on the ac frequency and border traps' locations into the oxide and should be independent of temperature [34].

For MOS systems with a very high D_{it} , the accumulation frequency dispersion can be a result of both interface states and border traps which makes the analysis more difficult. Border traps can also induce hysteresis behavior in the MOS capacitance-voltage (C-V) response, and this opens a new way to study the border traps and reveal a charge trapping density and how this varied with bias conditions, process changes and how the trapping evolves with time. Initial studies at the start of the PhD indicated that the charge trapping in border traps was comparable to, or even greater than, the typical interface state density values in high- k /III-V MOS systems [39]. However, the issue of C-V hysteresis in the high- k /III-V MOS system has received only a limited amount of research attention to date [40, 41]. As a result, the study of border traps using the C-V hysteresis technique formed a major aspect of the PhD research.

1.6 Thesis Outline

The main work of this thesis is to study the border traps and interface states in metal gate $\text{HfO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors using electrical characterization in order to gain an increased understanding of these defects in high- k /In_{0.53}Ga_{0.47}As MOS systems, and furthermore suggest possible routes to passivate these defects and thus reduce device instability. Chapter 2 will present the fundamental theories of MOS capacitors and the electrical measurements used for the characterization of the electrically active defects. Chapter 3 will discuss the primary study into the border traps using C-V hysteresis, placing an emphasis on the density of

trapped charge and its primary physical location in the oxide and how the trapped charge increases with the increasing stress bias. Chapter 4 studies how the trapped charge evolves with time for fixed stress bias and models the response based on charge trapping theories developed for high- k MOS systems on silicon. Chapter 5 reports on the effect of post-metal forming gas annealing (250°C to 450°C) on both the C-V hysteresis and interface states. The final experimental chapter, Chapter 6, introduces a combined study of C-V and hard x-ray photoelectron spectroscopy (HAXPES) on high- $k/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS structures for the accurate determination of Fermi level position at the oxide/semiconductor interface. Finally, the main findings of the PhD thesis are summarized in Chapter 7, along with some suggestions on how to extend the research work in this thesis.

Bibliography

- [1] G. E. Moore, *Electronics*, 38, (8), p. 114, (1965).
- [2] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices* (Wiley, NJ, 2007).
- [3] G. D. Wilk, R. M. Wallace, J. M. Anthony, *J. Appl. Phys.* **89**, 5243 (2001).
- [4] J. Robertson, *Rep. Prog. Phys.*, **69**, p. 327-396 (2006).
- [5] R. Engel-Herbert, Y. Hwang, and S. Stemmer, *J. Appl. Phys.* **108**, 124101 (2010).
- [6] R. M. Wallace, P. C. McIntyre, J. Kim, and Y. Nishi, *MRS Bulletin*, **34**, p493 (2009).
- [7] R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, and M. Metz, *IEEE Electron Device Lett.* **25**, 408 (2004).
- [8] K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M. Brazier, M. Buehler, A. Cappellani, R. Chau, C.-H. Choi, G. Ding, K. Fischer, T. Ghani, R. Grover, W. Han, D. Hanken, M. Hattendorf, J. He, J. Hicks, R. Huessner, D. Ingerly, P. Jain, R. James, L. Jong, S. Joshi, C. Kenyon, K. Kuhn, K. Lee, H. Liu, J. Maiz, B. McIntyre, P. Moon, J. Neiryneck, S. Pae, C. Parker, D. Parsons, C. Prasad, L. Pipes, M. Prince, P. Ranade, T. Reynolds, J. Sandford, L. Shifren, J. Sebastian, J. Seiple, D. Simon, S. Sivakumar, P. Smith, C. Thomas, T. Troeger, P. Vandervoorn, S. Williams, and K. Zawadzki, *Tech. Dig. - Int. Electron Devices Meet.* 247–250 (2007).
- [9] G. Groeseneken, L. Pantisano, L.-A. Ragnarsson, R. Degraeve, M. Houssa, T. Kauerauf, P. Roussel, S. De Gendt and M. Heyns, *Proceedings of the 11th IPFA*, p.147, Taiwan (2006).
- [10] M. Hiratani, S. Saito, Y. Shimamoto and K. Torii, *Japanese Journal of Appl. Phys.*, **41**, p. 4521, (2002).
- [11] R. D. Long, B. Shin, S. Monaghan, K. Cherkaoui, J. Cagnon, S. Stemmer, P. C. McIntyre, and P. K. Hurley, *J. Electrochem. Soc.* **158**, G103 (2011).
- [12] B. Shin, J. R. Weber, R. D. Long, P. K. Hurley, C. G. Van de Walle, and P. C. McIntyre, *Appl. Phys. Lett.* **96**, 152908 (2010).

- [13] E. H. Poindexter, *Semicond. Sci. Technol.* **4**, 961 (1989).
- [14] P. K. Hurley, A. Stesmans, V. V. Afanas'ev, B. J. O'Sullivan, and E. O'Callaghan, *J. Appl. Phys.*, **93**, 3971 (2003).
- [15] P. M. Lenahan and J. F. Conley, Jr., *J. Vac. Sci. Technol. B* **16**, 2134 (1998).
- [16] R. D. Long, E. O'Connor, S. B. Newcomb, S. Monaghan, K. Cherkaoui, P. Casey, G. Hughes, K. K. Thomas, F. Chalvet, I. M. Povey, M. E. Pemble, and P. K. Hurley, *J. Appl. Phys.* **106**, 084508 (2009).
- [17] J. Robertson, *Appl. Phys. Lett.*, **94**, 152104 (2010).
- [18] V. Djara, T. P. O'Regan, K. Cherkaoui, M. Schmidt, S. Monaghan, É. O'Connor, I. M. Povey, D. O'Connell, M. E. Pemble, and P. K. Hurley, *Microelectronic Engineering* **109**, 182 (2013).
- [19] D. P. Norton, *Mater. Sci. Eng. R* **43**, 139–247 (2004).
- [20] E. O'Connor, R. D. Long, K. Cherkaoui, K. K. Thomas, F. Chalvet, I. M. Povey, M. E. Pemble, P. K. Hurley, B. B. Brennan, G. Hughes, and S. Newcomb, *Appl. Phys. Lett.* **92**, 022902 (2008).
- [21] E. O'Connor, S. Monaghan, R. D. Long, A. O'Mahony, I. M. Povey, K. Cherkaoui, M. E. Pemble, G. Brammertz, M. Heyns, S. B. Newcomb, V. V. Afanas'ev, and P. K. Hurley, *Appl. Phys. Lett.* **94**, 102902 (2009).
- [22] G. Brammertz, H. C. Lin, M. Caymax, M. Meuris, M. Heyns, and M. Passlack, *Appl. Phys. Lett.* **95**, 202109 (2009).
- [23] P. K. Hurley, E. O'Connor, S. Monaghan, R. D. Long, A. O'Mahony, I. M. Povey, K. Cherkaoui, J. MacHale, A. J. Quinn, G. Brammertz, M. Heyns, S. B. Newcomb, V. V. Afanas'ev, A. M. Sonnet, R. V. Galatage, M. N. Jivani, E. M. Vogel, R. M. Wallace and M. E. Pemble, *ECS Trans.* **25**(6), 113 (2009).
- [24] Y. Hwang, R. Engel-Herbert, N. G. Rudawski, and S. Stemmer, *Appl. Phys. Lett.* **96**, 102910 (2010).
- [25] E. H. Nicollian and J. R. Brews, *MOS Physics and Technology* (Wiley, New York, 2003).
- [26] É. O'Connor, S. Monaghan, K. Cherkaoui, I. M. Povey, and P. K. Hurley, *Appl. Phys. Lett.* **99**, 212901 (2011).

- [27] V. Djara, K. Cherkaoui, M. Schmidt, S. Monaghan, E. O'Connor, I. M. Povey, D. O'Connell, M. E. Pemble, and P. K. Hurley, *IEEE Trans. Electron Devices* **59**(4), 1084–1090 (2012).
- [28] Q.-H. Luc, E. Y. Chang, H.-D. Trinh, H.-Q. Nguyen, B.-T. Tran, and Y.-C. Lin, *Jpn. J. Appl. Phys.* **53**, 04EF04 (2014).
- [29] S. Klejna and S. D. Elliot, *J. Phys. Chem. C* **116**(1), 643–654 (2012).
- [30] E. J. Kim, E. Chagarov, J. Cagnon, Y. Yuan, A. C. Kummel, P. M. Asbeck, S. Stemmer, K. C. Saraswat, and P. C. McIntyre, *J. Appl. Phys.* **106**, 124508 (2009).
- [31] S. Monaghan, A. O'Mahony, G. Provenzano, K. Cherkaoui, E. O'Connor, I. M. Povey, M. G. Nolan, D. O'Connell, S. B. Newcomb, F. Crupi, M. E. Pemble, and P. K. Hurley, *J. Vac. Sci. Technol. B* **29**(1), 01A807 (2011).
- [32] E. O'Connor, B. Brennan, V. Djara, K. Cherkaoui, S. Monaghan, S. B. Newcomb, R. Contreras, M. Milojevic, G. Hughes, M. E. Pemble, R. M. Wallace, and P. K. Hurley, *J. Appl. Phys.* **109**, 024101 (2011).
- [33] D. M. Fleetwood, M. R. Shaneyfelt, W. L. Warren, J. R. Schwank, T. L. Meisenheimer, and P. S. Winokur, *Microelectron. Reliab.* **35**, 403 (1995).
- [34] Y. Yuan, L. Wang, B. Yu, B. Shin, J. Ahn, P. C. McIntyre, P. M. Asbeck, M. J. W. Rodwell, and Y. Taur, *IEEE Electron Device Lett.* **32**(4), 485–487 (2011).
- [35] E. Simoen, D. H.-C. Lin, A. Alian, G. Brammertz, C. Merckling, J. Mitard, and C. Claeys, *IEEE Trans. Device Mater. Reliab.* **13**, 444 (2013).
- [36] C. Dou, D. Lin, A. Vais, T. Ivanov, H.-P. Chen, K. Martens, K. Kakushima, H. Iwai, Y. Taur, A. Thean, G. Groeseneken, *Microelectronics Reliability* **54**, 746–754 (2014).
- [37] M. Scarpino, S. Gupta, D. Lin, A. Alian, F. Crupi, N. Collaert, A. Thean, and E. Simoen, *IEEE Electron Device Lett.* **35**(7), 720–722 (2014).
- [38] J. Franco, A. Alian, B. Kaczer, D. Lin, T. Ivanov, A. Pourghaderi, K. Martens, Y. Mols, D. Zhou, N. Waldron, S. Sioncke, T. Kauerauf, N. Collaert, A. Thean, M. Heyns, and G. Groeseneken, *Tech. Dig. -Int. Reliab. Phys. Symp.* 2014, 6A.2.1.
- [39] J. Lin, Y. Y. Gomeniuk, S. Monaghan, I. M. Povey, K. Cherkaoui, É. O'Connor, M. Power and P. K. Hurley, *J. Appl. Phys.* **114**, 144105 (2013).

- [40] Y. Y. Gomeniuk, A. N. Nazarov, S. Monaghan, K. Cherkaoui, E. O'Connor, I. Povey, V. Djara, and P. K. Hurley, in Proceedings of the International Conference on nanomaterials: Applications and Properties (2012), vol. 1, no. 3, p. 03TF16.
- [41] N. Goel, D. Heh, S. Koveshnikov, I. Ok, S. Oktyabrsky, V. Tokranov, R. Kambhampati, M. Yakimov, Y. Sun, P. Pianetta, C. K. Gaspe, M. B. Santos, J. Lee, S. Datta, P. Majhi, and W. Tsai, Tech. Dig. - Int. Electron Devices Meet. 363–366 (2008).

Chapter 2: Theories and Measurement Techniques

2.1 Introduction

Metal-oxide-semiconductor capacitors (MOS capacitors) are used as the sample structure for all the research work presented in this thesis, and this chapter covers the basic theories behind the MOS device structure along with the resulting capacitance and conductance voltage responses and how they are influenced by interface states and border traps. Section 2.2 will discuss the basic operation of MOS capacitor, leakage mechanisms and an ideal capacitance-voltage (C-V) characteristic. Section 2.3 will focus on effect of fixed oxide charge, interface states and border traps on the electrical behavior of MOS capacitor. Section 2.4 will discuss the high-low frequency capacitance method and the conductance method for the extraction of interface state density. Section 2.5 will give the details of the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitor samples used in this work. Section 2.6 will conclude this chapter.

2.2 MOS System Characteristics

2.2.1 MOS Capacitor and Band bending

A MOS capacitor has a “sandwich” structure, consisting of metal gate, an oxide and semiconductor substrate as shown in Figure 2.1.

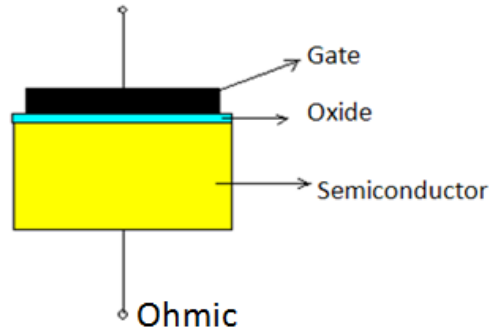


Figure 2.1: MOS capacitor structure.

In capacitance-voltage (C-V) and conductance-voltage (G-V) measurements, a slowly varying DC voltage is applied to the gate of the MOS capacitor and a small ac voltage is superposed on the gate bias in order to measure the capacitance and the conductance of the MOS capacitor as a function gate bias (V_g).

Mobile carriers in the semiconductor can be attracted to or repelled from the semiconductor surface by varying the DC gate voltage, thus the MOS capacitor is defined operating in different regions (i.e. accumulation, depletion and inversion) as shown in Figure 2.2 using a *p*-type MOS capacitor as an example.

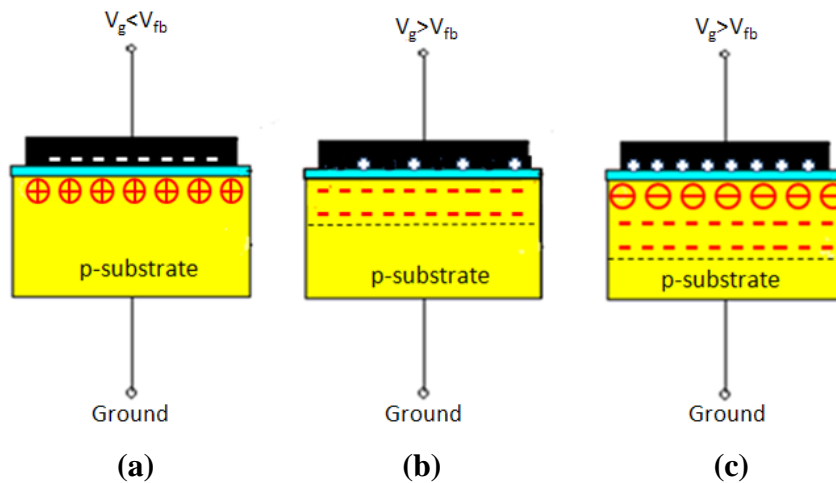


Figure 2.2: A *p*-type MOS capacitor operating in (a) accumulation (b) depletion and (c) inversion.

In order to understand the operation of MOS capacitor in different regions, the definitions of surface potential and bulk potential are introduced in the first place.

Band bending $\Psi(x)$ represents the potential at any point x in the semiconductor away from the semiconductor surface with respect to its value in the bulk and can be expressed as

$$\Psi(x) \equiv -\frac{E_i(x) - E_i(\infty)}{q} \quad (2.1)$$

where $E_i(x)$ is the intrinsic Fermi level at point x , $E_i(\infty)$ is the bulk intrinsic Fermi level and q is the elementary charge. Note that the Fermi level is defined as the energy level with the 50% possibility of being occupied by an electron. For intrinsic semiconductors, Fermi level is located in the middle of the bandgap (E_g), which is defined as the energy difference between the conduction band edge and valance band edge.

Surface potential, denoted as Ψ_s , is the total band bending (or the band bending at $x = 0$), and can be expressed as

$$\Psi_s \equiv \Psi(0) \equiv -\frac{E_i(0) - E_i(\infty)}{q} \quad (2.2)$$

where $E_i(0)$ is the surface intrinsic Fermi level.

Bulk potential, denoted as Φ_B , is defined as

$$\Phi_B \equiv \frac{E_f - E_i(\infty)}{q} \quad (2.3)$$

where, E_f is the Fermi level. For a given semiconductor doping level and temperature, Φ_B is a constant value and can be calculated by equation (2.4) based on Boltzman statistics.

$$|\Phi_B| \equiv \frac{k_B T}{q} \ln\left(\frac{N_{\text{doping}}}{n_i}\right) \quad (2.4)$$

where k_B is the Boltzmann constant ($k_B = 1.38 \times 10^{-23} \text{ JK}^{-1}$ or $8.617 \times 10^{-5} \text{ eV/K}$), T is the temperature in Kelvin [K], N_{doping} is the doping of the semiconductor in cm^{-3} and n_i is the intrinsic concentration of the semiconductor in cm^{-3} . Note that Φ_B is positive for n -type semiconductor and negative for p -type semiconductor.

The operation of p -type MOS capacitor can be represented by the band diagrams in Figure 2.3 and discussed in combination with the MOS structures in Figure 2.2.

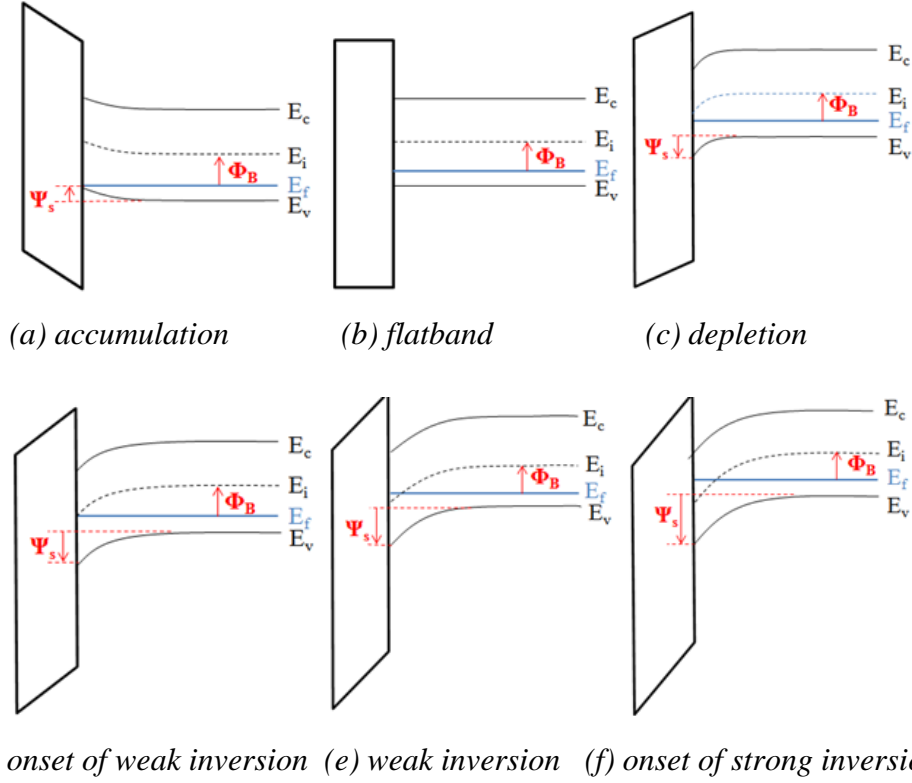


Figure 2.3: Band diagrams of a p -type MOS capacitor operating in (a) accumulation (b) flatband (c) depletion, (d) onset of weak inversion, (e) weak inversion, and (f) onset of strong inversion, where E_c represents conduction band minimum energy, E_v represents valance band maximum energy, E_f represents the Fermi level energy of the semiconductor and E_i represents the intrinsic Fermi level energy of the semiconductor.

In an ideal p -type MOS capacitor, by applying a gate voltage (V_g) that is smaller than the flatband voltage (the flatland voltage will be introduced later in this discussion) to the gate and thus creating negative charges in the gate, the majority carriers (holes) in the p -type substrate are attracted to the semiconductor surface as shown in Figure 2.2(a). The corresponding band diagram is illustrated in Figure 2.3(a). The semiconductor Fermi level is close to the valence band edge, indicating that holes are accumulated at the semiconductor surface (bands bending upward and thus $\Psi_s < 0$ according to

equation (2.2)). The hole density at the semiconductor surface becomes much greater than that in the bulk semiconductor. The p -type MOS capacitor is now operating in accumulation region.

As the gate voltage increases positively, there is a condition where the bands are flat throughout the semiconductor. This is called the flatband condition where $\Psi_s=0V$. The gate voltage that drives the MOS capacitor to flatband condition is called the flatband voltage denoted as V_{fb} . The band diagram of flatband condition is shown in Figure 2.3(b). For an ideal MOS capacitor, the flatband voltage equals to the work function difference between the metal and the semiconductor, which is denoted as Φ_{ms} , where the work function is defined as the smallest amount of energy needed to remove an electron from the Fermi level to vacuum level at absolute zero.

When the gate voltage increases beyond the flatband voltage, holes are repelled from the semiconductor surface, leaving a region depleted of mobile carriers. The p -type MOS capacitor operates in depletion. The depletion layer contains only the immobile negatively charged ions as shown in Figure 2.2(b). The band diagram of the p -type MOS capacitor operating in depletion illustrated in Figure 2.3(c) shows that the bands at semiconductor surface are bending downwards giving a positive value of Ψ_s , and the Fermi level at the semiconductor surface is still below the surface intrinsic Fermi level. As the Fermi level moves towards the intrinsic Fermi level at the semiconductor surface with the positively increasing V_g , the depletion layer width will increase.

As the gate voltage keeps increasing positively, minority carriers (electrons) are attracted to the semiconductor surface as shown in Figure 2.2(c). Another specific condition occurs when the Fermi level at the semiconductor surface crosses the surface intrinsic Fermi level, where the p -type MOS capacitor is referred to as being at the onset of weak inversion (Figure 2.3(d)). This condition is surface intrinsic with surface electron density equaling to surface hole density. At this stage, if the gate voltage keeps increasing positively, the surface Fermi level moves beyond the surface intrinsic Fermi level (Figure

2.3(e)), and there is a region referred to as weak inversion with increasing inversion charge (electrons) density at the semiconductor surface which is still less than the density of majority carriers in the bulk semiconductor.

Once the increasing surface potential Ψ_s becomes twice the value of the bulk potential (i.e. $\Psi_s = 2|\Phi_B|$), the MOS capacitor reaches the onset of strong inversion where the surface electron density becomes equal to the hole density in the bulk of semiconductor (Figure 2.3(f)). When the electron charge density at the surface increases greater than the hole density in the bulk ($\Psi_s > 2|\Phi_B|$), the p -type MOS capacitor is operating in strong inversion. In strong inversion, the Fermi level at the semiconductor surface is close to the conduction band edge, indicating the surface is strongly inverted by electrons. Once the MOS capacitor reaches strong inversion, the depletion layer width can hardly increase. Table 2.1 gives the full details of the semiconductor surface Fermi level position, surface potential and surface carrier density of the p -type MOS capacitor operating in different regions. The same theories can be applied to the n -type MOS capacitor by simply inverting the sign of the corresponding terms.

Table 2.1 Summary of MOS capacitor operating regions (for a p -type Si MOS structure)

Operating region	Surface E_f position	Surface potential	Surface carrier density
Accumulation	E_f is very close to E_v	$\Psi_s < 0V$	$p_s > N_a$
Flatband	$E_f - E_v = E_g/2 - q \Phi_B $	$\Psi_s = 0V$	$p_s = N_a$
Depletion	$E_g/2 > E_f - E_v > E_g/2 - q \Phi_B $	$0V < \Psi_s < \Phi_B $	$n_i < p_s < N_a$
Onset of weak inversion	E_f at midgap i.e. $E_f - E_v = E_g/2$	$\Psi_s = -\Phi_B > 0V$	$n_s = p_s = n_i$ i.e. surface intrinsic
Weak inversion	E_f is slightly above E_i $E_g/2 < E_f - E_v < E_g/2 + q \Phi_B $	$2 \Phi_B > \Psi_s > \Phi_B $	$n_i < n_s < N_a$
Onset of strong inversion	$E_f - E_v = E_g/2 + q \Phi_B $	$\Psi_s = -2\Phi_B > 0V$	$n_s = N_a$
Strong inversion	E_f is close to E_c $E_f - E_v > E_g/2 + q \Phi_B $	$\Psi_s > -2\Phi_B > 0V$	$n_s > N_a$

In Table 2.1:

N_a = doping level of the p -type semiconductor = hole density in the bulk of the p -type semiconductor

p_s = hole density at the semiconductor surface

n_s = electron density at the semiconductor surface

2.2.2 Leakage Mechanisms

In an ideal MOS capacitor, the oxide is a perfect insulator and the conductance of this insulating film is zero. In practice, however, there is always some level of leakage occurring. A few conduction mechanisms can attribute to the leakage through the oxide, such as direct tunnelling, Fowler-Nordheim tunnelling, thermionic emission, Frenkel-Poole emission, etc. Tunnelling is the most common conduction process that causes leakage under high electric fields. In this section, theory of direct tunnelling and Fowler-Nordheim tunnelling will be introduced.

The band diagram for direct tunnelling is illustrated in Figure 2.4(a), showing that the carriers can tunnel directly straight through the oxide. Direct tunnelling is significant in thin oxide (typically $< \sim 3\text{nm}$ for SiO_2) and the leakage (J_{DT}) caused by direct tunnelling is shown in equation (2.5).

$$J_{\text{DT}} = A \times E_{\text{ox}}^2 \times \exp\left(-\frac{B(1-(1-qV_{\text{ox}}/\phi_b)^{1.5})}{E_{\text{ox}}}\right) \quad (2.5)$$

where $A = \frac{q^3}{8\pi h \phi_b} \left(\frac{m}{m_{\text{ox}}}\right)$ (2.6)

and $B = \frac{8\pi \sqrt{2m_{\text{ox}} \phi_b^3}}{3qh}$ (2.7)

where h is Planck's constant, V_{ox} is the voltage drop across the oxide, E_{ox} is the oxide field, m_{ox} is the effective electron mass in the oxide, m is the free electron mass, and ϕ_b is the barrier height.

For Fowler-Nordheim tunnelling, carriers tunnel through only a partial width of the barrier as illustrated in Figure 2.4(b). Fowler-Nordheim tunnelling usually occurs in thicker oxides, and the leakage current (J_{FN}) caused by Fowler-Nordheim tunnelling is expressed in equation (2.8).

$$J_{\text{FN}} = AE_{\text{ox}}^2 \exp\left(-\frac{B}{E_{\text{ox}}}\right) \quad (2.8)$$

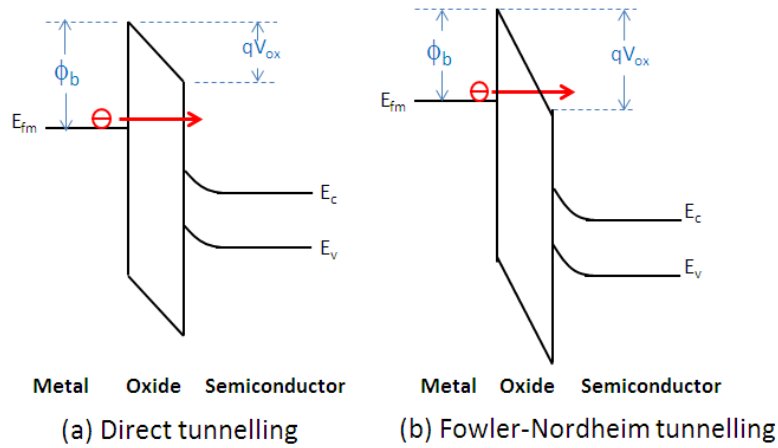


Figure 2.4: Band diagrams for leakage mechanism (a) Direct tunnelling and (b) Fowler-Nordheim tunnelling.

The temperature and voltage dependence of leakage current for a variety of conduction mechanisms is summarized in [1], which can be used to identify the leakage mechanisms that lead to the experimental gate current characteristics. It is noticeable in equations (2.5) and (2.8) that tunnelling leakage has a very strong dependence on the applied voltage and is independent on temperature. When the carriers are tunnelling through the oxide, defects can be generated in the oxide. Once these defects reach a density level that is enough to form a continuous chain connecting the gate to the semiconductor, a conduction path is created leading to catastrophic breakdown [1].

2.2.3 Ideal C-V Characteristic

The equivalent circuit of an ideal MOS capacitor consists of the oxide capacitance (see equation (1.2), $C_{ox} = \epsilon_0 k / t_{ox}$) in series with the differential capacitance of the semiconductor (C_s) and is shown in Figure 2.5.

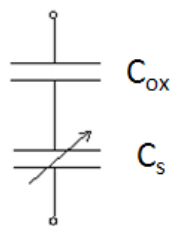


Figure 2.5: Equivalent circuit of an ideal MOS capacitor.

The total capacitance of the MOS capacitor is therefore expressed using equation (2.9).

$$\frac{1}{C_{\text{total}}} = \frac{1}{C_{\text{ox}}} + \frac{1}{C_s}$$

or

$$C_{\text{total}} = \frac{C_{\text{ox}} \times C_s}{C_{\text{ox}} + C_s} \quad (2.9)$$

where C_s is defined as the first derivative of the semiconductor surface charge (Q_s) with respect to the surface potential (Ψ_s) as expressed in equation (2.10).

$$C_s \equiv -\frac{dQ_s}{d\Psi_s} \quad (2.10)$$

Figure 2.6 illustrates C-V characteristic for ideal SiO_2/Si MOS capacitors. The equations used to obtain the C-V can be found in [1]. It is notable that the C-V demonstrates a symmetry behavior between strong accumulation and strong inversion. This is because the density of majority carrier is very large at the semiconductor surface in strong accumulation and the density of minority carrier is very large at the semiconductor surface in strong inversion, therefore C_s becomes very large compared to C_{ox} in both strong accumulation and strong inversion. According to equation (2.9), the total capacitance in either strong accumulation or strong inversion region is approximately equal to the oxide capacitance.

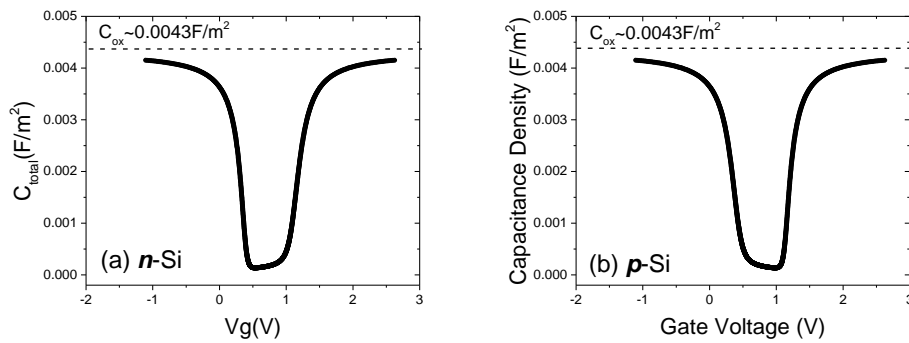


Figure 2.6: C-V characteristic for ideal (a) $\text{Ni}/\text{SiO}_2(8\text{nm})/\text{n-Si}$ and (b) $\text{Ni}/\text{SiO}_2(8\text{nm})/\text{p-Si}$ MOS capacitors. The plotted C-V curves are obtained from the calculations using equations in [1] based on Boltzman statistics. Doping used for Si is $1 \times 10^{15} \text{ cm}^{-3}$. Work function used for Ni is 5.37 eV.

In accumulation and depletion, the capacitance arises from the majority carriers that flow towards or away from the semiconductor surface following the applied ac voltage. Majority carriers respond immediately to the ac frequency used in our experiments (typically from 1kHz to 1MHz). Minority carriers, which play an important role and govern the C-V characteristic when the MOS capacitor is in inversion region, however, can only respond to low ac frequencies.

There are three mechanisms for getting the minority carriers including (1) generation of minority carriers from back contact, followed by diffusion through the quasi-neutral region of the semiconductor and then drift through the depletion layer to the inversion layer, (2) generation and recombination of minority carriers in the depletion layer and (3) supply from an inversion layer beyond the gate area [2]. In strong inversion, charge neutrality to the DC gate bias is satisfied by the increasing minority carriers near the semiconductor surface, and the depletion region width reaches a maximum. The inversion capacitance arises from the minority carriers that flow in and out of the inversion layer following the ac gate voltage. Once the supply of minority carriers that are controlled by any of the three mechanisms cannot keep up with the ac frequency, i.e. at very high frequencies, minority carriers will contribute no capacitance to the total capacitance of the MOS capacitor. Under this condition, majority carriers will flow into and away from the depletion layer edge as majority carriers respond immediately to the ac frequency. The depletion layer edge will move following the ac signal, and hence the measured capacitance is the depletion layer capacitance in series with the oxide capacitance. As the depletion layer width hardly changes in strong inversion, this results in a depletion layer capacitance that is an approximately constant value. Thus the measured capacitance at high frequency to which the minority cannot respond at all is a constant value that is independent of gate bias and is the lowest of the entire C-V in strong inversion region. At intermediate frequencies, the minority carrier can respond to the ac frequency to some extent, and the capacitance measured at such frequencies is intermediate between the low and high frequency capacitances. The lower the ac frequency is, the higher the capacitance

contributed by minority carrier is measured. Therefore, the measured C-V will exhibit a frequency dispersion behavior.

Figure 2.7 is an example showing the frequency dispersion in inversion. It has to highlight that for an ideal MOS system measured at all frequencies, the capacitance should be a constant value and independent of gate bias in strong inversion. In addition to the dependence of minority carriers on frequency, measurement temperature and bandgap of the semiconductor can also affect the minority carrier response thus further affect the C-V in inversion region. Either a lower temperature or a larger bandgap can make the minority carrier response time longer thus suppresses the minority carrier response and reduces the measured inversion capacitance.

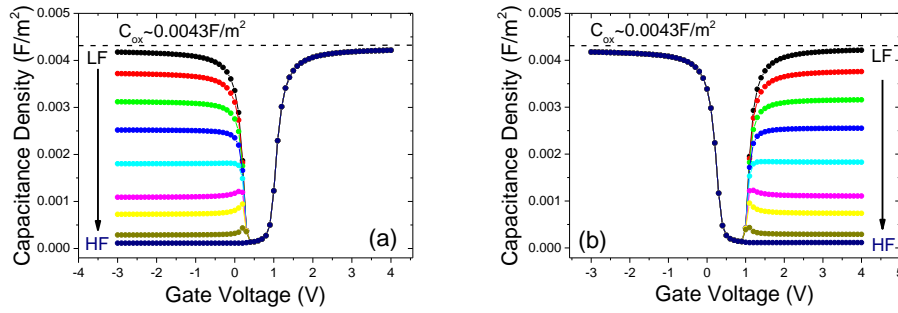


Figure 2.7: Simulated multi-frequency C-V responses for ideal (a) Ni/SiO₂(8nm)/n-Si and (b) Ni/SiO₂(8nm)/p-Si MOS capacitors that exhibit frequency dispersion in inversion region because minority carriers cannot respond to the increasing ac frequency. The simulation is performed using Silvaco Device Simulator. Doping used for Si is $1 \times 10^{15} \text{ cm}^{-3}$. Work function used for Ni is 5.37eV.

For In_{0.53}Ga_{0.47}As MOS capacitor, an asymmetry in the C-V is obtained due to the low density of states in the conduction band ($N_c = 2.1 \times 10^{17} \text{ cm}^{-3}$) compared to the valance band density of states ($N_v = 7.7 \times 10^{18} \text{ cm}^{-3}$) [3]. A simulated C-V for an ideal high- k /n-In_{0.53}Ga_{0.47}As MOS capacitor is illustrated in Figure 2.8, showing that the capacitance in accumulation is noticeably lower than that in inversion, resulting from the low value of N_c . However, this asymmetry is usually not observed in experiments due to the

interface states located inside the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ conduction band [4, 5], which will be discussed in the next section.

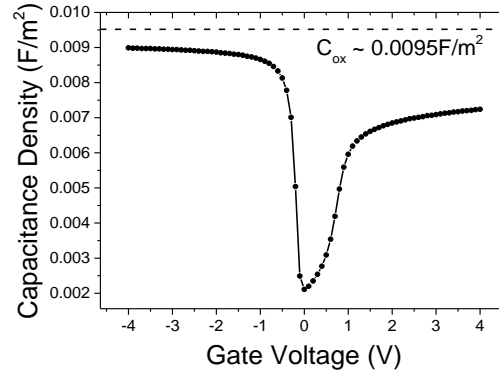


Figure 2.8: Simulated C-V responses at a low frequency of 20Hz for an ideal $\text{Ni}/\text{Al}_2\text{O}_3(8\text{nm})/\text{n-In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitor that exhibits an asymmetry in the capacitance in the inversion and accumulation region. The simulation is performed using Silvaco Device Simulator. Doping used for $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ is $4 \times 10^{17} \text{cm}^{-3}$. Work function used for Ni is 5.37eV.

2.3 Non-ideal MOS Capacitor and the Characterization of Defects

Fixed oxide charge

Fixed oxide charge (Q_f) that exists in the bulk oxide or near the oxide/semiconductor interface can affect C-V response by shifting the C-V in a parallel direction along the gate voltage axis as shown in Figure 2.9. Positive Q_f shifts C-V negatively and negative Q_f shifts C-V positively.

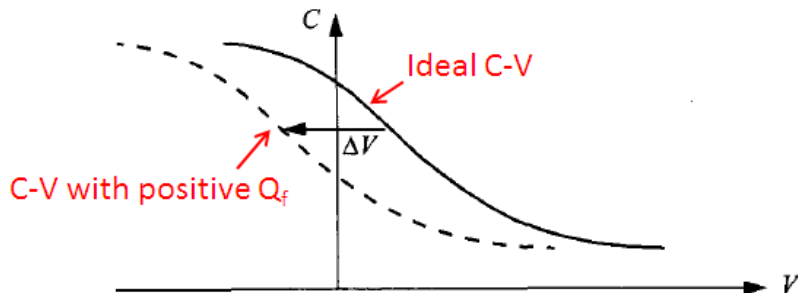


Figure 2.9: Parallel C-V shift due to fixed oxide charges [1].

Interface states

Interface states introduce extra energy levels within the semiconductor bandgap and can be divided into donor-type and acceptor-type interface states [6]. Donor-type (+/0) interface states are neutral when their energy levels are positioned below the Fermi level being occupied by electrons, and are positively charged when the energy levels are above the Fermi level in which case they are empty. Acceptor-type (0/-) interface states are neutral when empty and are negatively charged when filled with electrons. The interface states can exchange charges with the semiconductor bands following the ac frequency during the C-V measurements and therefore give rise to a capacitance (see Figure 2.10). The equivalent circuit of a MOS capacitor with oxide/semiconductor interface states is shown in Figure 2.11, where C_{it} is the capacitance associated with the interface states.

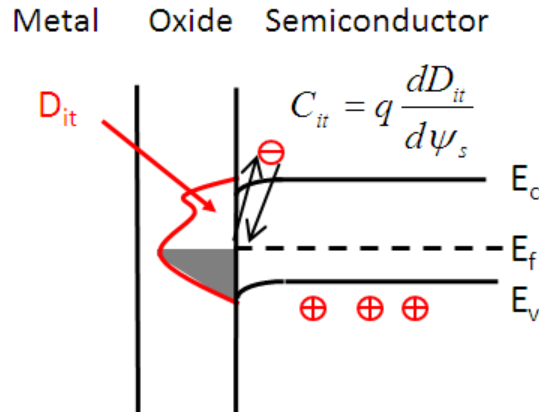


Figure 2.10: Band diagram for MOS capacitor with interface states.

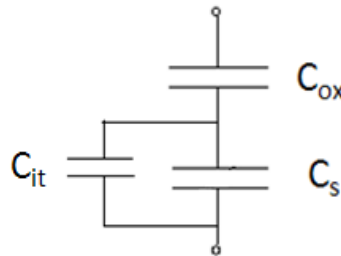


Figure 2.11: Equivalent circuit of a MOS capacitor with C_{it} .

The total capacitance of the MOS capacitor becomes

$$\frac{1}{C_{total}} = \frac{1}{C_{ox}} + \frac{1}{C_s + C_{it}} \quad (2.11)$$

In high- k /In_{0.53}Ga_{0.47}As MOS systems, an interfacial layer can be formed between the high- k oxide and In_{0.53}Ga_{0.47}As, adding an extra capacitance (C_{IL}) to the gate stack as shown in Figure 2.12. The total capacitance of the MOS capacitor becomes shown in equation (2.12) when both the interface states capacitance and interface layer capacitance are taken into consideration.

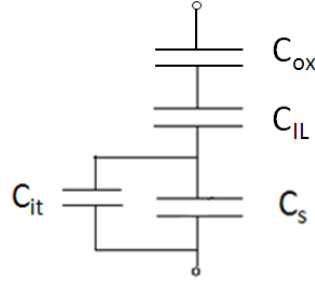


Figure 2.12: Equivalent circuit of a MOS capacitor with C_{IL} and C_{it} .

$$\frac{1}{C_{total}} = \frac{1}{C_{ox}} + \frac{1}{C_{IL}} + \frac{1}{C_s + C_{it}} \quad (2.12)$$

Interface states are frequency dependent. C-V characteristic at high frequencies to which interface states cannot respond at all will only be stretched out along the gate voltage axis due to the DC filling or emptying of the interface state energy levels. At low frequencies, the ideal C-V is distorted due to the combination of stretch-out along the gate voltage and the addition of C_{it} component to the overall capacitance. Figure 2.13 shows how the C-V with interface states deviate from the ideal C-V at both low and high frequencies. Theoretically interface states located near the semiconductor band edges have very fast response time, therefore the capacitance measured in near accumulation should be only weakly dependent on frequency over the range of typical ac measurement frequencies (20Hz to 1MHz). However, for measurements at radio frequencies and/or low temperature, these interface states can be detected.

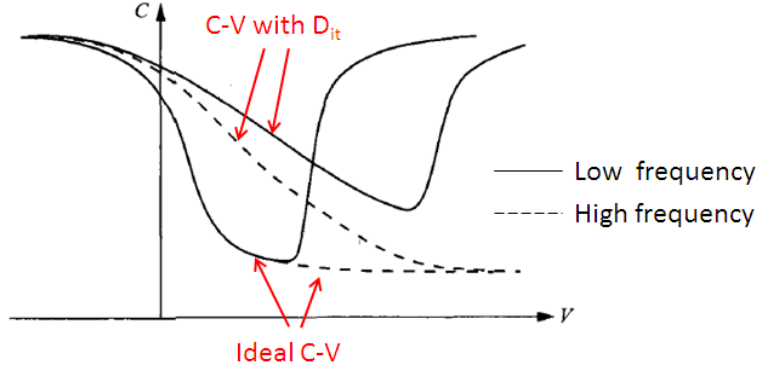


Figure 2.13: C-V with and without the presence of interface states [1].

Another way in which interface states can manifest themselves is the “ C_{it} bumps”, which arise from the Fermi level going through a peak interface state density in the bandgap as shown in Figure 2.14 using SiO_2/Si structure as an example. In a typical high- $k/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS system, there is a distribution of D_{it} across the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ bandgap; therefore the “ C_{it} bumps” are observed to be wider than that shown in Figure 2.14. Moreover, the D_{it} distribution extends to the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ conduction band. As the conduction band density of state is small in $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, the Fermi level can go further into the conduction band and can interact with D_{it} inside the conduction band. This result in an addition of C_{it} component to the measured capacitance in accumulation for $n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitor, and therefore the measured accumulation capacitance can be close to C_{ox} as opposed to the theoretical C-V illustrated in Figure 2.8.

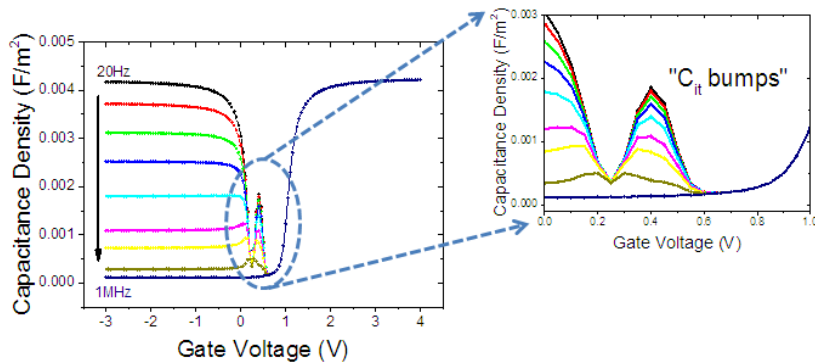


Figure 2.14: Simulated multi-frequency C-V responses for a $\text{Ni}/\text{SiO}_2(8\text{nm})/n\text{-Si}$ MOS capacitor with the presence of a single energy level interface state ($D_{it}=2 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$) at 0.35 eV above the valence band edge.

In addition to the frequency dependence, interface state response is also temperature dependent. For the case of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS system, if the C-V measurements are carried out at very low temperatures (typically -50°C), the response of interface states will be suppressed, thus C_{it} term becomes approximately to zero. The equivalent circuit of a MOS capacitor at high frequency and/or low temperature where no interface states respond at all ($C_{it}=0$) is the same to the equivalent circuit of an ideal MOS capacitor (see Figure 2.5) if C_{IL} is not accounted for. However, the gate voltage for each surface potential is changed due to the charging of interfaces states, which will stretch out the C-V along the gate voltage axis as discussed earlier (see Figure 2.13).

Border traps

Border traps can be located in the oxide near the oxide/semiconductor interface. Using an n -type MOS capacitor as an example in Figure 2.15, the electrons can tunnel into the charge trapping sites when the n -type MOS capacitor is in accumulation with its Fermi level close to the conduction band edge and aligned with the border trap energy levels. The electrons will tunnel into or be emitted from the border traps following the ac movement of the semiconductor Fermi level. The time constant associated charge exchange between border traps and conduction band increases exponentially with the depth into the oxide. Therefore, for the case of border traps distributed into the oxide, this will induce a frequency dependent capacitance in accumulation, where the dispersion has been observed to extend over a very wide range of frequencies (from 20Hz to above 1GHz).

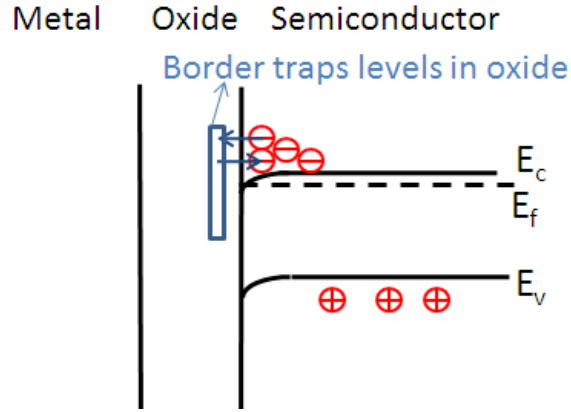


Figure 2.15: Band diagram for an n-type MOS capacitor with oxide border traps near the oxide/semiconductor interface which exchange charges with the semiconductor conduction band via a direct tunnelling process.

Border traps have been examined using the accumulation frequency dispersion for $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS system as reported in [7], showing that this frequency dispersion is independent of temperature which is consistent with a tunnelling process and not attributed to the temperature dependent interface states. However, for a MOS system with a much higher D_{it} such as $\text{HfO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ structure, the accumulation frequency dispersion is not purely contributed by border traps. Figure 2.16 illustrates the measured multi-frequency C-V responses for $\text{Pd}/\text{HfO}_2(10\text{nm})/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitor, which is one of the MOS structures in the PhD studies, showing the level of frequency dispersion in accumulation has a dependence on temperature, consistent with the interface states response near the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ band edges. For $\text{HfO}_2/p\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$, the variation of accumulation frequency dispersion with temperature is wider than the case of $n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$, indicating a very high D_{it} distribution in the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ lower bandgap or near the valence band edge that causes the frequency dispersion in addition to the effect of border traps.

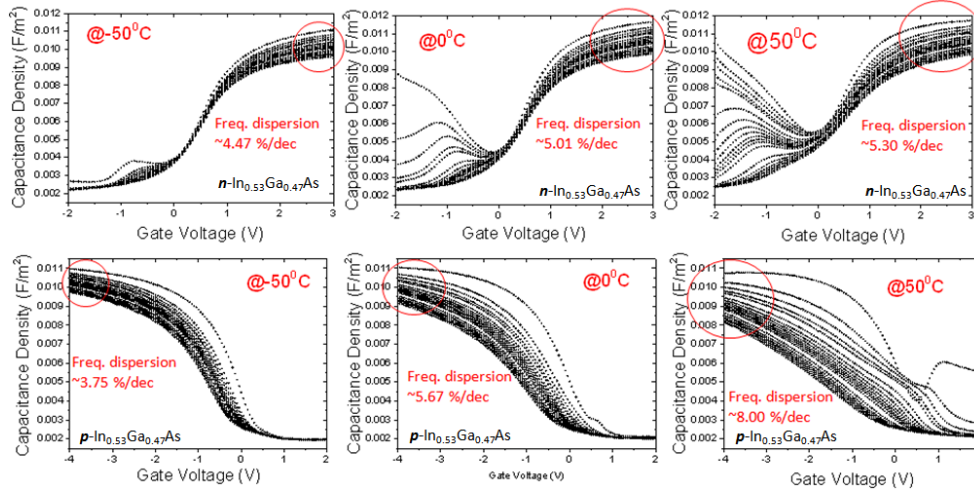


Figure 2.16: Measured multi-frequency (1kHz~1MHz) C-V responses for Pd/HfO₂(10nm)/In_{0.53}Ga_{0.47}As MOS capacitor, showing a temperature dependent frequency dispersion in accumulation for both n-type and p-type In_{0.53}Ga_{0.47}As.

In addition to causing accumulation frequency dispersion in the measured capacitance, charge trapping sites located in the oxide can be manifest as hysteresis in the C-V response. Figure 2.17 illustrates a C-V hysteresis process for an n-type MOS capacitor where the C-V is swept from inversion upward to accumulation and subsequently swept downward to inversion. The hysteresis window arises from electrons tunnelling into the border traps when the Fermi level is aligned with their energy levels in accumulation region and filling the border trap energy levels that are below the Fermi level. During the downward C-V direction where the Fermi level is moving away from the conduction band edge, those electrons trapped in the border traps cannot be moved away unless the Fermi level is moved close to the valance band edge (more discussion in Chapter 3) thus resulting in a voltage shift (or C-V hysteresis). The charge trapping density can be quantified using the C-V hysteresis measurement and equation (2.13) assuming all the trapped charges are located near/at the oxide/semiconductor interface.

$$Q_{\text{trapped}} = \frac{\Delta V \times C_{\text{ox}}}{q} \quad (2.13)$$

where Q_{trapped} is the density of trapped charge in cm⁻², ΔV is the C-V hysteresis window in V, C_{ox} is the oxide capacitance in F/cm², and q is the elementary charge in Coulombs [C]. In this thesis, ΔV is estimated at flatland

capacitance (C_{fb}), half the maximum capacitance in accumulation ($C_{max}/2$), or the mid-point capacitance along the C-V sweep, providing that the C-V hysteresis is approximately a parallel shift. The C-V hysteresis can be representative of only border traps by ruling out the contribution from interface states as the effect of D_{it} should be the same in both upward and downward directions of the C-V sweep. Therefore, any C-V shift due to C_{it} is cancelled out when extracting the voltage shift between the upward C-V and downward C-V.

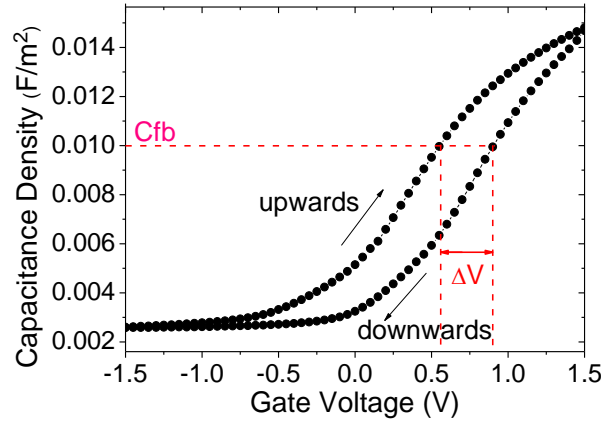


Figure 2.17: C-V hysteresis for a Pt/HfO₂(5nm)/n-In_{0.53}Ga_{0.47}As MOS capacitor.

Conclusions of the effect of fixed oxide charges, interface states and border traps on C-V

To conclude, interface states, fixed oxide charges and border traps are defects in MOS capacitors that can induce flatband voltage instability and distort the ideal C-V characteristics. In an ideal MOS system, the flatband voltage equals to the metal and semiconductor work function difference. Taking into consideration the defects, the flatband voltage then becomes

$$V_{fb} = \Phi_{ms} - \frac{Q_{it}}{C_{ox}} - \frac{Q_f}{C_{ox}} - \frac{Q_{ot}}{C_{ox}} \quad (2.14)$$

where Φ_{ms} is the work function difference between the metal and semiconductor, Q_{it} is the incorporated interface charge at the flatband condition, Q_f is amount of fixed charges in the oxide, Q_{ot} is the charges trapped at border traps [1].

For SiO₂/Si MOS systems, the defect density is small therefore the C-V responses are very similar to the theoretical behavior, which is not the case for high-*k*/III-V MOS systems. Figure 2.18 illustrates measured multi-frequency (1k-1MHz) C-V responses for a Pd/HfO₂(10nm)/*n*-In_{0.53}Ga_{0.47}As MOS capacitor. The measured C-V behavior represents the electrically active defects in a range of ways listed below based on the discussions from earlier.

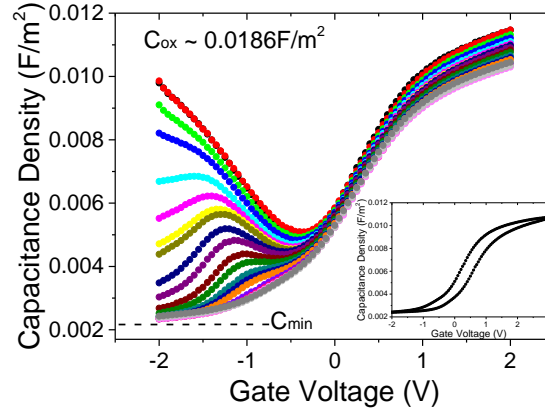


Figure 2.18: Experimental multi-frequency (1kHz-1MHz) C-V responses at room temperature for a Pd/HfO₂(10nm)/*n*-In_{0.53}Ga_{0.47}As MOS capacitor. Inset is the measured C-V hysteresis at 1MHz.

(1) An interfacial oxide layer with a much lower *k*-value between HfO₂ and In_{0.53}Ga_{0.47}As can be formed. This will result in an extra capacitance (*C*_{IL}) in series with the oxide capacitance from HfO₂ alone (~0.0186F/m² using a *k*-value of 21 [8]), thus reducing the overall capacitance.

(2) The asymmetry (i.e. lower capacitance in accumulation than that in inversion for *n*-In_{0.53}Ga_{0.47}As) in the C-V is not observed due to the interface states inside the conduction band which add *C*_{it} component to the total capacitance.

(3) The C-V responses are stretched out due to the addition of *C*_{it} to the measured capacitance and the DC filling and emptying of the interface states when the Fermi level is going through the bandgap.

(4) There is a frequency dispersion in accumulation attributed to border traps with energy levels near the conduction band edge. The border traps also induce C-V hysteresis shown in inset.

(5) The measured capacitance in inversion has wide and large peaks resulting from D_{it} in the lower bandgap as opposed to a constant capacitance with bias (i.e. “plateau region”) which is expected for an ideal inverted surface (see Figure 2.7 and Figure 2.8).

(6) The whole C-V response is shifted due to the combination of fixed oxide charges, interface states and charge trapping (see equation (2.14)).

The above analysis indicates that the high- k /III-V MOS system is very complicated in terms of interpreting the experimental C-V behavior. It is very important to separate the effect of fixed charges, interface states and border traps and thus to look at these defects individually, understand their nature and furthermore find the methods to passivate these defects in order to reduce device instability.

2.4 Extraction of D_{it} Using High-Low Frequency Capacitance Method and Conductance Method

2.4.1 High-Low Frequency Capacitance Method

For both the high frequency capacitance-voltage method [1, 2, 9] and low frequency C-V method [1, 2, 10] (not discussed in this thesis), the extraction of interface state density (D_{it}) requires a comparison between the measured C-V and the theoretical/simulated C-V which limits the accuracy of the D_{it} extraction because there are two major uncertainties when calculating the theoretical C-V, namely the doping concentration of the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ substrate and the oxide capacitance [11]. The high-low frequency (HF-LF) capacitance method was developed by R. Castagne and A. Vapaille [1, 2, 12] who suggested combining the measured C-V at a low frequency to which the interface states can completely respond and the measured C-V at a high frequency to which the interface states cannot respond at all. This method thus eliminates the need for the calculation for a theoretical C-V. It is noted that at both low and high frequencies, the interface states respond to the slowly varying DC bias which result in a stretch-out along the V_g axis. Figure 2.19 illustrates the equivalent circuits of MOS capacitor measured at (a) low frequency ($C_{it} \neq 0$) and (b) high frequency ($C_{it} = 0$).

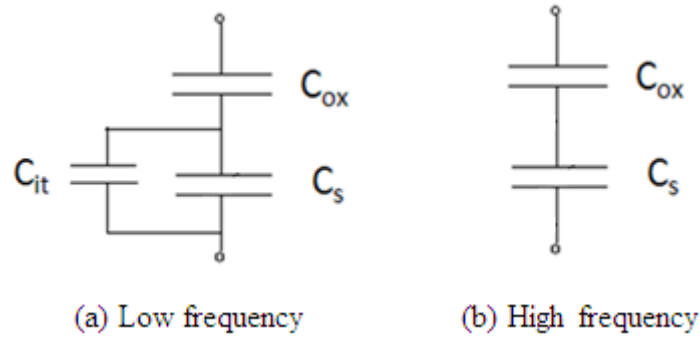


Figure 2.19: Equivalent circuit of MOS capacitor measured at (a) low frequency and (b) high frequency.

The low frequency capacitance (C_{LF}) according to Figure 2.19(a) can be written as

$$\frac{1}{C_{LF}} = \frac{1}{C_{ox}} + \frac{1}{C_s + C_{it}} \quad (2.15)$$

Rearranging equation (2.15) yields

$$C_{it} = \frac{C_{ox}C_{LF}}{C_{ox} - C_{LF}} - C_s \quad (2.16)$$

where C_s can be estimated from the high frequency capacitance (C_{HF}) and according to Figure 2.19(b). C_s is expressed as

$$C_s = \frac{C_{ox} \times C_{HF}}{C_{ox} - C_{HF}} \quad (2.17)$$

Substituting equation (2.17) to equation (2.16) yields

$$C_{it} = \left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}} \right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}} \right)^{-1} \quad (2.18)$$

The interface state density (D_{it}) can be expressed as

$$D_{it} = \frac{C_{it}}{q} = \frac{1}{q} \times \left[\left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}} \right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}} \right)^{-1} \right] (\text{cm}^{-2}\text{eV}^{-1}) \quad (2.19)$$

where C_{it} is in F/cm^2 , q is the elementary charge in Coulomb [C], and D_{it} is thus in unit of $\text{cm}^{-2}\text{eV}^{-1}$.

Caution must be taken when using HF-LF capacitance method to extract D_{it} by avoiding using the capacitance measured in the regions where minority carrier interaction with interface states occurs, or where minority carriers resulting through bulk minority carrier generation or diffusion of minority carriers from the quasi-neutral bulk occurs, as this additional capacitance could induce errors in the calculated D_{it} values. Using the measured low and high frequency C-V for an Au/Ni/ $\text{Al}_2\text{O}_3(8\text{nm})/n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS

capacitor as an example (Figure 2.20), the capacitance measured at 20Hz is significantly affected by the minority carrier responses in inversion ($V_g \approx -0.5V$ to $-3V$), and in the case of accumulation region ($V_g \approx 1.5V$ to $2.8V$), both 20Hz and 1MHz capacitance are contributed by the majority carrier response as majority carries have very fast response times. In both regions, using the low and high frequency capacitance can lead to a large error in D_{it} . Therefore, it is crucial to use the HF-LF capacitance method in depletion.

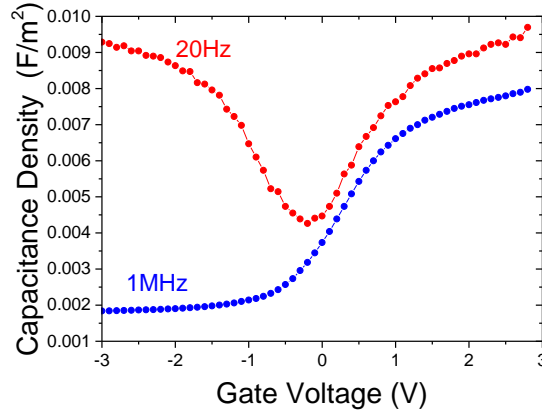


Figure 2.20: Measured low and high frequency C-V at room temperature for an Au/Ni/Al₂O₃(8nm)/n-In_{0.53}Ga_{0.47}As MOS capacitor.

In practice, the extracted D_{it} can have errors as the measured 1MHz C-V is not the true high frequency C-V with C_{it} component being non-zero especially in high D_{it} system such as high- k /In_{0.53}Ga_{0.47}As MOS systems. An optimum way to obtain true high frequency C-V is to carry out the measurement at a sufficiently low temperature (e.g. 77K [13]) in order to suppress the interface state response to a greater extent. There is a limitation of the lowest temperature that can be reached in most test labs. An alternative way to obtain a true high frequency C-V is to do a simulation of a C-V with no C_{it} contributions based on some parameters extracted from the experimental C-V, which is not covered in this thesis.

When it comes to the step of calculating D_{it} using equation (2.19), the uncertainty in C_{ox} still exists which can cause big errors in D_{it} extraction. Estimation of C_{ox} using the maximum capacitance (C_{max}) in accumulation is

often used; however this is not applicable to $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS systems due to the low conduction band density of states, in which case C_{max} is much lower than C_{ox} but C_{max} can also be increased due to the D_{it} inside the conduction band. S. Monaghan *et al* [14] proposed a C_{ox} extraction method by analyzing (G_{m}/ω) versus $\log \omega$ curve in strong inversion where the value of G_{m}/ω goes through a peak (i.e. $(G_{\text{m}}/\omega)_{\text{max}}$) at a transition frequency, where G_{m} is the measured conductance and ω is the ac frequency in rad/s. One can estimate C_{ox} using the value of $(G_{\text{m}}/\omega)_{\text{max}}$ (for details refer to [14]).

2.4.2 Conductance Method

The conductance method was developed by E. H. Nicollian and A. Goetzberger [15] and is the most popular D_{it} extraction method used in many research groups. The conductance of a MOS capacitor can physically arise from the oxide leakage, or the loss due to a bulk generation and recombination process, or the loss associated with the change in the occupancy of interface state energy levels with variations in ac frequencies. Using the conductance method to extract D_{it} , one has to make sure that the oxide leakage is low enough so that the leakage won't contribute to the conductance. When a small ac voltage is applied to the gate of a MOS capacitor, the occupancy of the interface state energy level is changed in a small energy interval (\sim a few $k_{\text{B}}T/q$ wide) centered about the Fermi level due to majority carriers being captured or emitted following the ac frequencies. The capture and emission of majority carriers by interface states result in an energy loss observed at all frequencies except the very lowest frequency to which interface states respond immediately and the very highest frequency to which interface states cannot respond at all. This results in a frequency dependent parallel conductance/frequency (G_{p}/ω) behavior for interface states (will be discussed later in this section), which can be distinguished from a bulk generation and recombination process induced conductance. The conductance method is only valid in depletion region where the minority carrier response is negligible.

G-V

During the measurement of the capacitance as a function of gate bias, the conductance can be measured as a function of gate bias (G-V). In the G-V responses, the peaks in conductance are usually observed which correspond to the peak in the interface state density, which is also reflected by the “bumps” that are observed in the C-V responses. Figure 2.21 illustrates experimental multi-frequency (1kHz to 1MHz) C-V and G-V responses for an Al/SiO₂(8nm)/n-Si MOS capacitor, where the interface states associated capacitance and conductance peaks are noticeably in the same bias range at $V_g = -1V$ to $-0.25V$. It is also noted that minority carrier response in inversion is not observed in this sample due to the larger bandgap of silicon (1.12eV) compared to In_{0.53}Ga_{0.47}As (0.75eV). It is important to perform the conductance method in such a bias region where peaks in conductance and peaks in capacitance both occur.

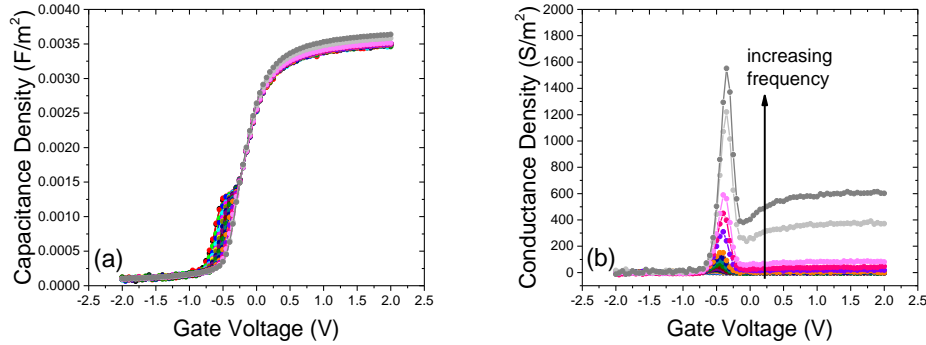


Figure 2.21: Measured multi-frequency (1kHz to 1MHz) (a) C-V and (b) G-V responses for an Al/SiO₂(8nm)/n-Si MOS capacitor, showing the interface states associated capacitance and conductance peaks.

G_p/ω versus ω at a fixed V_g

Figure 2.22 illustrates the equivalent circuits of MOS capacitor in measurement mode and the components of the measured circuit model for the extraction of D_{it} . The conductance method is based on the analysis of the equivalent parallel conductance, based on Figure 2.22, G_p/ω is expressed as

$$\frac{G_p}{\omega} = \frac{\omega C_{ox} G_m}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \quad (2.20)$$

where G_p is the parallel conductance representing the total loss associated with the MOS capacitor, ω is the radian frequency, C_{ox} is the oxide capacitance, C_m is the measured capacitance and G_m is measured conductance. One can extract the G_p/ω versus log frequency profile from a traditional C-V/G-V measurement during which the capacitance and conductance are measured as a function of V_g by sweeping the V_g at a fixed frequency and repeating for a series of frequencies. This can however stress the samples and create more interface defects. An alternative way is to measure the capacitance and conductance by sweeping the frequency in a log scale at a fixed V_g and then repeating the same process for a series of V_g values in depletion, which reduces the density of stress induced interface states.

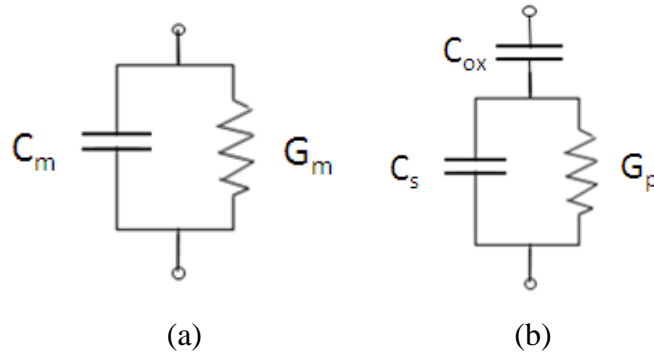


Figure 2.22: (a) equivalent circuit of MOS capacitor in measurement mode (b) the components of the measured circuit model.

For D_{it} analysis, G_p/ω versus log frequency f or ω , where f is the applied ac frequency in Hz and ω is the radian frequency ($\omega=2\pi f$) in rad/s, is generated for a series of V_g values in depletion. Figure 2.23 shows the G_p/ω as a function of frequency f (Hz) at different gate bias points for a $\text{SiO}_2/n\text{-Si}$ MOS structure as published by Nicollian and Brews [2], illustrating G_p/ω goes through a peak value, i.e. $(G_p/\omega)_{\max}$, at a certain frequency denoted as f_p , over the ac frequency range which is plotted in natural logarithmic scale.

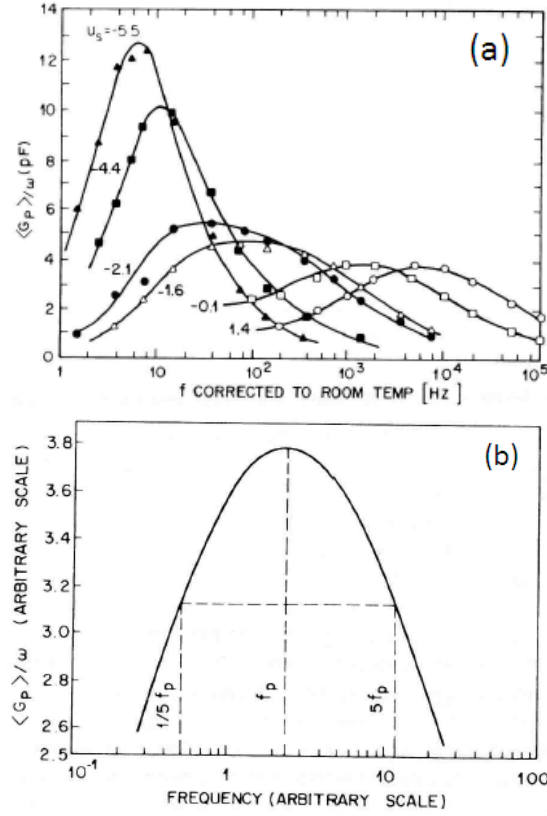


Figure 2.23: (a) G_p/ω as a function of frequency at different gate bias points for a SiO₂/n-Si MOS structure as published by Nicollian and Brews [2]. (b) A typical G_p/ω versus log frequency curve showing the width [2].

The cause of a peak in G_p/ω value in the G_p/ω versus log frequency curve is explained as follows. A fixed gate voltage corresponds to a particular band bending (or surface potential) and thus a particular majority carrier density at the substrate surface. This majority carrier density determines the capture rate of the interface states. The (G_p/ω) peak occurs when the majority carrier capture rate by the interface states becomes comparable to the applied ac frequency. The loss will be reduced when interface states respond faster to the decreasing ac frequency and also when it becomes harder for interface states to respond as ac frequency is increasing. These result in the peak in G_p/ω observed. In terms of the $(G_p/\omega)_{\max}$ values varying with the applied V_g as shown in Figure 2.23, there is a specific V_g value in depletion that gives a larger $(G_p/\omega)_{\max}$ value than that given by other V_g values, and the $(G_p/\omega)_{\max}$ value is smaller when the applied V_g corresponds to MOS capacitor being in further into accumulation or further into depletion. This is because the

majority carrier density is very large in accumulation resulting in a very rapid interface state capture rate compared to the applied ac frequency thus less loss occurs, and further into depletion, the majority carrier density is reduced which slows down the interface state capture rate to the extent that very small amount of interface states can respond. In both cases, the loss associated with interface states is reduced; therefore the value of G_p/ω is smaller.

A universal function ($f_d(\sigma_s)$) of the standard deviation of the surface potential (σ_s) is introduced below [2].

$$f_d(\sigma_s) = \frac{(2\pi\sigma_s^2)^{-1/2}}{2\xi_p} \int_{-\infty}^{\infty} \exp\left(-\frac{\eta^2}{2\sigma_s^2}\right) \exp(-\eta) \ln(1 + \xi_p^2 \exp(2\eta)) d\eta \quad (2.21)$$

where $\eta = v_s - \langle v_s \rangle$, $\langle v_s \rangle$ is the mean value of band bending, $\xi_p = \tau_p \omega_p$, $\omega_p = 2\pi f_p$, and τ_p is the trapping time constant.

The analysis is usually based on the estimation of the ratio of amplitude change in the G_p/ω value in the G_p/ω versus log frequency curve either between f_p and $5f_p$ or between f_p and $0.2f_p$ as shown in Figure 2.23(b). In other words, the value of either of the two terms as shown below has to be extracted from the G_p/ω versus log frequency curve:

$$\frac{(G_p/\omega)_{5f_p}}{(G_p/\omega)_{f_p}} \text{ or } \frac{(G_p/\omega)_{0.2f_p}}{(G_p/\omega)_{f_p}}$$

This value is then used to obtain the standard deviation of substrate band bending (σ_s). Once σ_s is known, $f_d(\sigma_s)$ can be determined. Details of the calculation of σ_s and $f_d(\sigma_s)$ can be found in [2] and will not be discussed in this thesis. Once $f_d(\sigma_s)$ is determined, the interface state density D_{it} is calculated using equation (2.22).

$$D_{it} = \frac{1}{(f_d(\sigma_s) \times q)} \times \left(\frac{G_p}{\omega}\right)_{\max} \quad (2.22)$$

For the ease of D_{it} analysis, the standard deviation of the substrate band bending (σ_s) is assumed to be zero, which yields a value of 0.4 for $f_d(\sigma_s)$ [2, 11]. Equation (2.22) thus becomes

$$D_{it} = \frac{2.5}{q} \times \left(\frac{G_p}{\omega}\right)_{\max} \quad (2.23)$$

The conductance method is only accurate for MOS systems with $qD_{it} < C_{ox}$. If $qD_{it} > C_{ox}$, the measured impedance will be dominated by C_{ox} and D_{it} can be underestimated [11]. Moreover, when qD_{it} becomes so large that $qD_{it} > 4C_{ox}$, the extracted G_p/ω will become insensitive to the interface states and even no peak values of G_p/ω can be found in the G_p/ω versus log frequency curves [11]. The determination of the energy level of interface states requires the Berglund integral which can be found elsewhere [1, 2] and is out of the scope of this thesis.

2.5 Experimental High- k /In_{0.53}Ga_{0.47}As MOS Capacitor Structures

Due to the combination of a high electron mobility ($\sim 14,000 \text{ cm}^2/\text{Vs}$ at low doping levels), suitable energy gap ($\sim 0.75 \text{ eV}$) and the fact that it can be grown lattice matched in InP, there has been a considerable focus of research attention on In_xGa_{1-x}As with a 53% In concentration (i.e. In_{0.53}Ga_{0.47}As), and In_{0.53}Ga_{0.47}As was used as the channel substrate for all the MOS capacitors under investigation. The structure for the experimental MOS capacitors used in this work is shown in Figure 2.24.

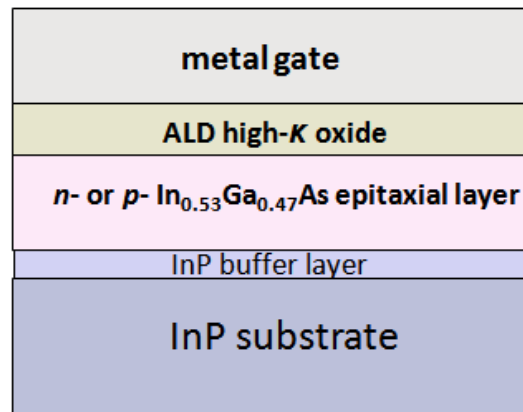


Figure 2.24: Sample structure used for the work presented in this thesis. High enough doping in the InP substrate ensures a good ohmic contact across the entire area to the chuck.

The samples used in this work were heavily n -doped (S at $\sim 2 \times 10^{18} \text{ cm}^{-3}$) and heavily p -doped (Zn at $\sim 2 \times 10^{18} \text{ cm}^{-3}$) InP(100) substrates with $2 \mu\text{m}$ n -type (S at $\sim 4 \times 10^{17} \text{ cm}^{-3}$) and p -type (Zn at $\sim 4 \times 10^{17} \text{ cm}^{-3}$) In_{0.53}Ga_{0.47}As epitaxial layers

respectively, grown by metal organic vapour phase epitaxy (MOVPE). The $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ surfaces were initially degreased by sequentially rinsing for 1min each in acetone, methanol, and isopropanol. Before the high- k oxide deposition, the samples were immersed in $(\text{NH}_4)_2\text{S}$ solutions (10% in deionized H_2O) for 20 min at room temperature ($\sim 295\text{K}$). The 10% $(\text{NH}_4)_2\text{S}$ passivation approach for 20 minutes and room temperature was found to be the optimum to suppress the formation of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ native oxides and to reduce the high- $k/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface state density as reported in [16]. Samples were then introduced to the atomic layer deposition (ALD) chamber load lock (base pressure of less than $2 \times 10^{-5}\text{mbar}$) after the removal from the 10% $(\text{NH}_4)_2\text{S}$ surface passivation solution. The transfer time from the aqueous $(\text{NH}_4)_2\text{S}$ solution to the ALD chamber was kept to a minimum (typically 3min) in order to minimize the formation of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ native oxides due to air exposure.

Both HfO_2 and Al_2O_3 were used as the high- k oxide in this work. The HfO_2 was deposited by ALD using $\text{Hf}[\text{N}(\text{CH}_3)\text{C}_2\text{H}_5]_4$ (TEMAH) and H_2O as precursors at 250°C . The Al_2O_3 was deposited by ALD at either 250°C and 300°C using trimethylaluminum (TMA) $\text{Al}(\text{CH}_3)_3$ and H_2O . In this work we examined samples with several metal gates (i.e. Pt, Pd, Ni/Au and Al) representing low and high work functions. Gate contacts were formed by electron beam evaporation and a lift-off process. Figure 2.25 illustrates a top down view of a die that has square shaped MOS capacitors with a range of areas. MOS capacitors with areas from $30\mu\text{m} \times 30\mu\text{m}$ to $100\mu\text{m} \times 100\mu\text{m}$ were used in this study. One of the high- $k/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ sample sets presented in this thesis used TiN as the metal gate which was deposited by sputtering and patterned using lift-off in IMEC (see Chapter 5).

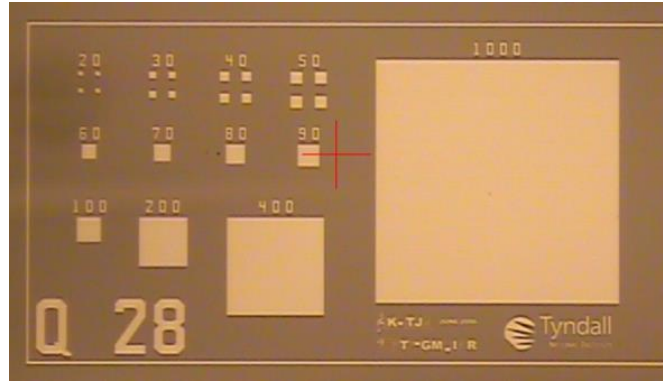


Figure 2.25: Fabricated capacitor structures from a top down view for a die with various MOS capacitor areas. Cross sectional structure of these fabricated MOS capacitor has been shown in Figure 2.24.

The electrical measurements were performed using a Cascade Microtech probe station (model Submit 12971B) in a dry air, dark environment. Current-voltage (I-V) measurements were carried out using either an HP4156 or an Agilent B1500A semiconductor device analyzer prior to any C-V/G-V measurements in order to obtain the bias range that can be applied without the risk of breaking down the MOS capacitors. The C-V and G-V measurements were recorded using either an Agilent CV-enabled B1500A or an E4980 LCR meter. Multiple sites with different capacitor areas on each sample wafer were examined to ensure the I-V, C-V and G-V characteristics presented in this thesis are representative of the sample behavior.

2.6 Conclusions

An overview of MOS capacitor theories is introduced based on band bending and C-V characteristics in this chapter. Fixed oxide charges, interface states and border traps have their own signatures in the electrical characteristics (C-V, G-V and G_p/ω), which can help to distinguish the various charged defect responses in experimental data, which is especially important in case of the high defect density values which are typically present in high- k /In_{0.53}Ga_{0.47}As MOS systems.

Bibliography

- [1] S. M. Sze and K. K. Ng, Physics of Semiconductor Devices (Wiley, NJ, 2007).
- [2] E. H. Nicollian and J. R. Brews, MOS Physics and Technology (Wiley, New York, 2003).
- [3] <http://www.ioffe.rssi.ru/SVA/NSM/Semicond/GaInAs/bandstr.html>
- [4] G. Brammertz, H. C. Lin, M. Caymax, M. Meuris, M. Heyns, and M. Passlack, Appl. Phys. Lett. **95**, 202109 (2009).
- [5] N. Taoka, M. Yokoyama, S. H. Kim, R. Suzuki, R. Iida, S. Lee, T. Hoshii, W. Jevasuwan, T. Maeda, T. Yasuda, O. Ichikawa, N. Fukuhara, M. Hata, M. Takenaka, and S. Takagi, in Proceedings of the IEEE International Electron Devices Meeting-IEDM (IEEE, 2011), p. 610.
- [6] R. D. Long, B. Shin, S. Monaghan, K. Cherkaoui, J. Cagnon, S. Stemmer, P. C. McIntyre, and P. K. Hurley, J. Electrochem. Soc. **158**, G103 (2011).
- [7] E. J. Kim, L. Wang, P. M. Asbeck, K. C. Saraswat, and P. C. McIntyre, Appl. Phys. Lett. **96**, 012906 (2010).
- [8] K. Cherkaoui, S. Monaghan, M. A. Negara, M. Modreanu, P. K. Hurley, D. O'Connell, S. McDonnell, G. Hughes, S. Wright, R. C. Barklie, P. Bailey, and T. C. Q. Noakes, J. Appl. Phys. **104**, 064113 (2008).
- [9] L. M. Terman, Solid-State Electron. **5**, 285(1962).
- [10] M. Kuhn, Solid-State Electron. **13**, 873(1970).
- [11] R. Engel-Herbert, Y. Hwang, and S. Stemmer, J. Appl. Phys. **108**, 124101 (2010).
- [12] R. Castagne and A. Vapaille, Surf. Sci., **28**, 157 (1971).
- [13] P. K. Hurley, E. O'Connor, S. Monaghan, R. D. Long, A. O'Mahony, I. M. Povey, K. Cherkaoui, J. MacHale, A. J. Quinn, G. Brammertz, M. Heyns, S. B. Newcomb, V. V. Afanas'ev, A. M. Sonnet, R. V. Galatage, M. N. Jivani, E. M. Vogel, R. M. Wallace and M. E. Pemble, ECS Trans. **25**(6), 113 (2009).
- [14] S. Monaghan, E. O'Connor, R. Rios, F. Ferdousi, L. Floyd, E. Ryan, K. Cherkaoui, I. M. Povey, K. J. Kuhn and P. K. Hurley, IEEE Trans. Electron Devices, **61**(12), 4176–4185 (2014).
- [15] E. H. Nicollian and A. Goetzberger, Bell Syst. Tech. J., **46**, 1055 (1967).

[16] E. O'Connor, B. Brennan, V. Djara, K. Cherkaoui, S. Monaghan, S. B. Newcomb, R. Contreras, M. Milojevic, G. Hughes, M. E. Pemble, R. M. Wallace, and P. K. Hurley, *J. Appl. Phys.* **109**, 024101 (2011).

Chapter 3: An Investigation of C-V Hysteresis in Metal/High- k /In_{0.53}Ga_{0.47}As MOS Capacitors

3.1 Introduction

Charge trapping states can be located in the transition region between the high- k oxide and In_{0.53}Ga_{0.47}As surface in MOS systems and are often referred to as “slow states” or “border traps”. These trapping sites have been examined based on the dispersion they cause in the capacitance with ac signal frequency for In_{0.53}Ga_{0.47}As MOS structures biased in accumulation [1-4]. However, this dispersion can also include fast interface states aligned with energy levels in the In_{0.53}Ga_{0.47}As conduction band [5, 6], which complicates analysis of border traps based on the frequency dispersion of the accumulation capacitance. In addition to causing frequency dispersion in the measured capacitance, charge trapping sites located in the oxide can be manifest as hysteresis in the C-V response. The issue of C-V hysteresis in the In_{0.53}Ga_{0.47}As MOS system has received only a limited amount of research attention to date [7, 8]. The issue of C-V hysteresis is important from a technological perspective as it represents a physical process that results in device instability, and in addition, the level of charge trapping can be comparable to, or even greater than the effect of interface states for the In_{0.53}Ga_{0.47}As MOS system.

From a scientific perspective, the study of C-V hysteresis is of interest as it presents a method to analyze and quantify the density of charge trapping states in high- k oxides on III-V surfaces. The principal aim of the work in

this chapter is to investigate C-V hysteresis in the high- k /In_{0.53}Ga_{0.47}As MOS system for different metal gate electrodes and varying experimental bias conditions in order to quantify the level of electron and hole trapping, and to gain a more complete understanding of the primary location of the charge trapping sites. The experimental results also provide insight into the approach that is required to reduce the density of charge trapping sites responsible for the C-V hysteresis in the In_{0.53}Ga_{0.47}As MOS system.

Section 3.2 will detail the experimental samples used for the C-V hysteresis studies along with the measurement details. The primary investigation into C-V hysteresis behavior will be discussed in section 3.3. Section 3.4 will give further insight into the origin of the C-V hysteresis and section 3.5 will analyze the distribution of the trapped charge in the high- k oxide based on an oxide thickness series. Section 3.6 will conclude the whole chapter.

3.2 Experimental Details

Both n -doped and p -doped In_{0.53}Ga_{0.47}As epitaxial layers were used as the channel substrate in order to investigate both electron and hole trapping using MOS samples biased towards accumulation. The In_{0.53}Ga_{0.47}As surfaces were treated using the optimised 10% (NH₄)₂S solution prior to ALD plus a minimum transfer time to the ALD chamber [9]. Either HfO₂ or Al₂O₃ were deposited on the In_{0.53}Ga_{0.47}As by ALD. The HfO₂ dielectric has a nominal thickness of 5nm by ALD using Hf[N(CH₃)C₂H₅]₄ (TEMAH) and H₂O as precursors at 250⁰C. The Al₂O₃ dielectric has a nominal thickness of 8nm and was deposited by ALD at 300⁰C using trimethylaluminum (TMA) Al(CH₃)₃ and H₂O. For the Al₂O₃ thickness series results presented in this work, the Al₂O₃ dielectric with nominal thicknesses of 5, 10, 15, 20nm were deposited by ALD at 250⁰C using TMA and H₂O. For the HfO₂ thickness series investigated, the HfO₂ with nominal thicknesses of 10, 15, 20, 25, 30nm were deposited by ALD at 250⁰C using the TEMAH and H₂O. In this work, we examined samples with several metal gates representing low and high work functions, which included Al, Pt, Pd, and Ni/Au. Gate contacts were formed by electron beam evaporation and a lift-off process. Pt(115nm)

and Al(115nm) were used as the two metal gates for HfO₂(5nm) samples, Al(160nm) and Ni(70nm)/Au(90nm) were the two gates for Al₂O₃(8nm) samples, and Pd(160nm) was the metal gate for both the Al₂O₃ thickness series (5~20nm) and the HfO₂ thickness series (10~30nm). The full sample details are provided in Table 3.1.

Table 3.1 Samples details for C-V hysteresis study

Sample	Gate (thickness)	Oxide (thickness)	ALD precursors	ALD temperatures
HfO ₂ /In _{0.53} Ga _{0.47} As sample series	Pt (115nm)	HfO ₂ (5nm)	TEMAH and H ₂ O	250°C
	Al (115nm)	HfO ₂ (5nm)		
Al ₂ O ₃ /In _{0.53} Ga _{0.47} As sample series	Ni/Au (70nm/90nm)	Al ₂ O ₃ (8nm)	TMA and H ₂ O	300°C
	Al (160nm)	Al ₂ O ₃ (8nm)		
HfO ₂ /In _{0.53} Ga _{0.47} As oxide thickness series	Pd (160nm)	HfO ₂ (10, 15, 20, 25, 30nm)	TEMAH and H ₂ O	250°C
Al ₂ O ₃ /In _{0.53} Ga _{0.47} As oxide thickness series	Pd (160nm)	Al ₂ O ₃ (5, 10, 15, 20nm)	TMA and H ₂ O	250°C

The C-V hysteresis measurements were recorded using a Cascade Microtech probe station (model Submit 12971B) and an Agilent CV-enabled B1500A semiconductor device analyzer. All the C-V hysteresis measurements were carried out at a high frequency of 1MHz and at room temperature (295K) in order to minimize the contribution of high-*k*/In_{0.53}Ga_{0.47}As interface states to the overall capacitance (i.e. C_{it}≈0). Under these conditions, the primary effect of the interface states is to stretch out the measured high frequency C-V along the gate voltage axis [10, 11].

All the reported C-V hysteresis responses were measured starting from inversion and sweeping towards the accumulation region, and subsequently sweeping back towards inversion. There was no hold time in accumulation. The terms “inversion” and “accumulation” used here are for simplicity of expression to represent the nominal regions of the C-V characteristic. To confirm surface inversion would require more analysis, but this is beyond the scope of the research work reported in this study. The MOS capacitors under

investigation were all driven beyond the flatband condition and towards accumulation region which allows charge to be accumulated at the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ surface. The C-V hysteresis (i.e. the gate voltage difference between the double-directional sweeps) is estimated at either the flat-band capacitance (C_{fb}) or half the maximum capacitance in accumulation ($C_{\text{max}}/2$). The level of charge trapping is quantified using the following equation:

$$Q_{\text{trapped}} = \frac{\Delta V \times C_{\text{ox}}}{q} \text{ (cm}^{-2}\text{)} \quad (3.1)$$

where Q_{trapped} is the population of trapped charge in cm^{-2} , ΔV is the C-V hysteresis in V, C_{ox} is the oxide capacitance in F/cm^2 (proportional to the oxide k -value and inversely proportional to the oxide thickness), and q is the elementary charge in Coulombs [C]. The value of Q_{trapped} in equation (3.1) represents the equivalent charge density at the oxide/ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface. The effect of different oxide electric fields due to small variations in oxide thickness has been neglected. The C_{ox} values are based on oxide thickness values obtained from high-resolution cross-sectional transmission electron microscopy (HR-TEM), taking into account any interfacial oxide layers formed in the MOS structure. The following dielectric constant values were adopted, HfO_2 (21) [12], Al_2O_3 (8.6) [7] and the native oxide of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ (9) [13, 14]. These values will also be used for the other chapters of this thesis.

3.3 Primary Investigation into C-V Hysteresis

Twenty C-V hysteresis sweeps for n -type and p -type $\text{Pt/HfO}_2(5\text{nm})/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors are shown in Figures 3.1(a) and 3.1(b), respectively. The flat-band voltage (V_{fb}) difference estimated from the first C-V hysteresis sweep, which is shown in black stars in Figure 3.1, corresponds to an electron trapping level of $4.7 \times 10^{12} \text{cm}^{-2}$ for the n -type sample, and a hole trapping level of $1.6 \times 10^{13} \text{cm}^{-2}$ for the p -type sample, assuming all the charge trapping is taking place at the $\text{HfO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface. The validity of this assumption will be explored later in section 3.4. The density calculations are based on an oxide capacitance value of $C_{\text{ox}} = 2.5 \times 10^{-6} \text{F/cm}^2$ taking into consideration the $\text{HfO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface oxide thickness observed in the TEM micrographs which will be presented

and discussed later. Both the electron and hole trapping levels are comparable to the estimated interface state density (D_{it}) using the approach described in [15], highlighting the importance of electron and hole trapping in the high- k /In_{0.53}Ga_{0.47}As MOS system.

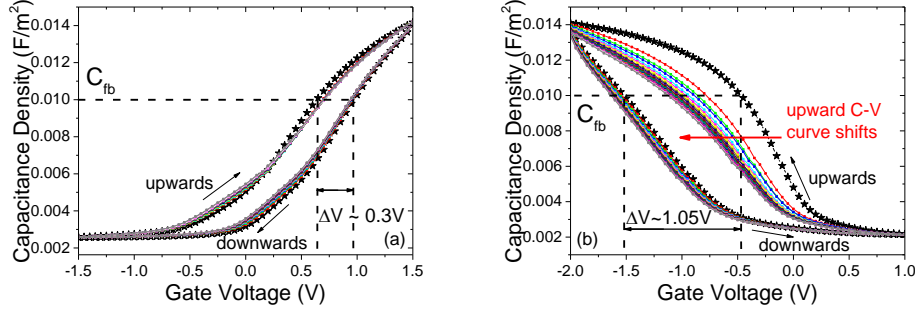


Figure 3.1: Twenty C-V hysteresis responses at 1MHz and 295K for (a) Pt/HfO₂(5nm)/n-In_{0.53}Ga_{0.47}As/n-InP and (b) Pt/HfO₂(5nm)/p-In_{0.53}Ga_{0.47}As/p-InP MOS capacitors. A progressive gate voltage shift occurring with subsequent C-V sweeps is evident in the upward sweep direction in (b). Note: the curve with black star symbols is the 1st C-V hysteresis sweep.

Considering first the n -type In_{0.53}Ga_{0.47}As sample in Figure 3.1(a), the repeated C-V hysteresis sweeps are almost overlapping the 1st C-V hysteresis in the upward sweep direction, where the MOS capacitor is measured from inversion to accumulation, indicating that the majority of charge trapping is a reversible process (or a temporary trapping behavior). In the p -type In_{0.53}Ga_{0.47}As sample (Figure 3.1(b)), there is a significant shift in V_{fb} between the 1st and 2nd C-V hysteresis sweeps, but subsequent sweeps show the same behavior as the n -type sample, where the majority of the charge trapping is a reversible process. There is only a small non-reversible component referred to here as “permanent” charge trapping, which is manifested as a progressive shift in V_{fb} in the inversion to accumulation sweeps of the C-V responses, which is a positive V_{fb} shift for the n -type sample and a negative V_{fb} shift for the p -type sample. From Figure 3.1, it is clear that the progressive V_{fb} shift is more significant in the p -type sample, implying a larger portion of permanently trapped charges in the p -type sample compared to that in the n -type sample.

Figure 3.2 illustrates the effect of the maximum bias in accumulation on the level of C-V hysteresis. For these measurements, the same starting DC bias point in inversion is used, with an increasing maximum DC bias point in accumulation (V_{\max}) for the Pt/HfO₂(5nm)/*n*-In_{0.53}Ga_{0.47}As (Figure 3.2(a)) and Pt/HfO₂(5nm)/*p*-In_{0.53}Ga_{0.47}As (Figure 3.2(b)) MOS capacitors. As shown in the insets of the figures, the C-V hysteresis window increases linearly with V_{\max} . Note that all the C-V hysteresis measurements (with increasing V_{\max}) for both *n*- and *p*-type sample were performed on the same device on each wafer therefore the upward C-V shift can also play a role in the C-V hysteresis window shown in Figure 3.2 (especially in the case of *p*-type sample). The C-V hysteresis is also found to increase with V_{\max} for the Al₂O₃(8nm)/In_{0.53}Ga_{0.47}As MOS structures, but the level of increase is less than observed for the HfO₂ structures (results not shown).

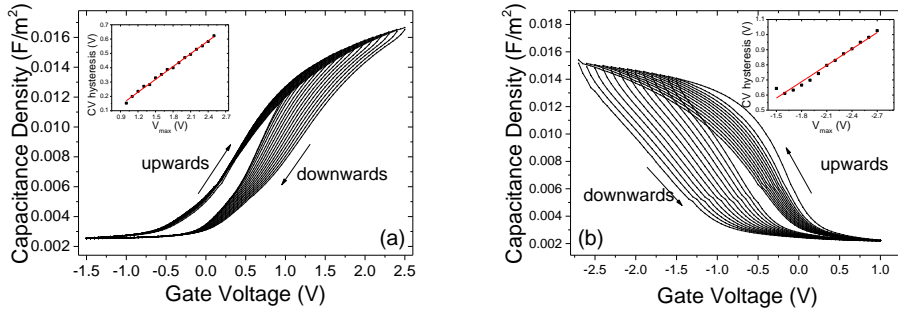


Figure 3.2: C-V hysteresis at 1MHz and 295K for (a) Pt/HfO₂(5nm)/*n*-In_{0.53}Ga_{0.47}As and (b) Pt/HfO₂(5nm)/*p*-In_{0.53}Ga_{0.47}As MOS capacitors using the same start DC bias in inversion and increasing DC bias (V_{\max}) in accumulation. Inset is the C-V hysteresis as a function of V_{\max} .

It has recently been demonstrated that SiO₂ doped HfO₂ [16] and ZrHfO₂ thin films on silicon [17] exhibit a ferroelectric behavior. The direction of the C-V hysteresis loops in Figures 3.2(a) and 3.2(b) obtained for the undoped HfO₂ are not consistent with a ferroelectric response, suggesting electron and hole trapping as the source of the C-V hysteresis.

As C-V hysteresis has a dependence on the maximum bias values in accumulation, it is crucial to keep the oxide field the same (i.e. the same

$|V_{\max}-V_{fb}|/t_{ox})$ when comparing the C-V hysteresis between different samples. The same oxide field results in the same density of majority carriers accumulated at the oxide/ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface during the stress. From Figure 3.2, it is possible to compare the level of charge trapping in the n - and p -type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ samples at the same maximum electric field across the oxide. For example, if $|V_{\max}-V_{fb}|$ is taken as 1.4V, the trapped charge density is $7.3 \times 10^{12} \text{cm}^{-2}$ for the $n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ sample and $1.3 \times 10^{13} \text{cm}^{-2}$ for the $p\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS sample, where the Q_{trapped} for the $p\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ can be underestimated because the corresponding C-V sweep is not the first sweep measured on that device in which case there is a large positive V_{fb} shift. The effect of “permanent” charge trapping for $n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ also exists but is much less noticeable than $p\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$. These indicate that there is a significantly lower level of charge trapping in the case of the n -type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitor than in the case of $p\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$. There are a range of possible factors which can contribute to the higher level of temporary charge trapping (i.e. C-V hysteresis) and permanent charge trapping in the $p\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS structures, which are illustrated schematically by the energy band diagrams shown in Figures 3.3(a) and 3.3(b) for the n -type and p -type samples, respectively. The possible reasons for a higher level of charge trapping in the p -type sample compared to the n -type sample are: (i) a higher density of border traps with energy levels aligned with the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ valance band edge than that aligned with the conduction band edge, (ii) the barrier height ΔE_v for the trapped holes tunnelling in and out of the border traps is larger than the barrier height ΔE_c for the electron tunnelling [18].

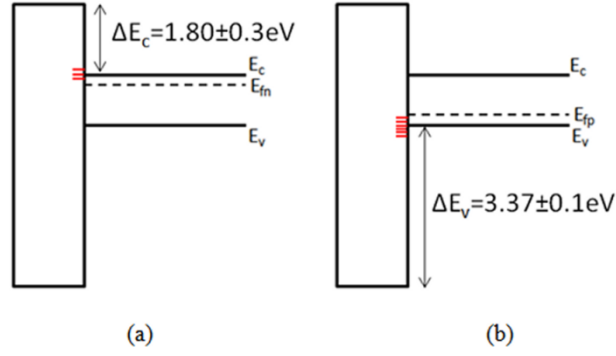


Figure 3.3: Band diagrams for (a) $\text{HfO}_2/\text{n-In}_{0.53}\text{Ga}_{0.47}\text{As}$ and (b) $\text{HfO}_2/\text{p-In}_{0.53}\text{Ga}_{0.47}\text{As}$ structures [18]. The energy levels shown in red are the border trap energy levels which are aligned with the conduction band edge (E_c) for the n-type sample and aligned with the valance band edge (E_v) for the p-type sample.

3.4 Impact of Gate Metal on C-V Hysteresis

The study of the C-V hysteresis also included an examination of the impact of the metal gate based on low (i.e. aluminium) and high (i.e. platinum) work function metals, as detailed in Table 3.1. Figure 3.4 shows the C-V hysteresis for the $\text{Pt}/\text{HfO}_2(5\text{nm})/\text{n-In}_{0.53}\text{Ga}_{0.47}\text{As}$ and $\text{Al}/\text{HfO}_2(5\text{nm})/\text{n-In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors. The Al gate sample is driven into strong accumulation as the measured capacitance is plateauing at 1.5V, and the value of $|V_{\text{max}} - V_{\text{fb}}|$ is higher for the Al gate samples than the Pt gate sample. Under this condition, the C-V responses exhibit three features of importance. First, the maximum capacitance in accumulation (C_{max}) for the Al gate sample is almost half of that obtained for the Pt gate sample. Second, the level of charge trapping determined from the C-V hysteresis at the flat-band capacitance for the Al gate sample, of $6.8 \times 10^{11} \text{cm}^{-2}$, is significantly lower when compared to $4.7 \times 10^{12} \text{cm}^{-2}$ for the Pt gate sample. In addition, the reduced charge trapping for the Al gate sample occurs even with a higher value of $|V_{\text{max}} - V_{\text{fb}}|$. Finally, the samples exhibit a low level of frequency dispersion in the region corresponding to nominal accumulation as shown in Figure 3.5 for (a) Pt and (b) Al gate samples. In addition, the capacitance in this bias region does not significantly change when reducing the temperature to -50°C . These results suggest the samples exhibit genuine surface accumulation [19].

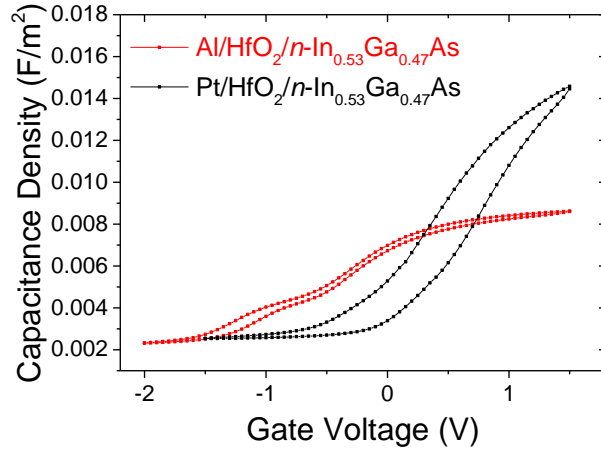


Figure 3.4: C-V hysteresis at 1MHz and 295K for Pt/HfO₂(5nm)/n-In_{0.53}Ga_{0.47}As and Al/HfO₂(5nm)/n-In_{0.53}Ga_{0.47}As MOS capacitors. There is a significant reduction in the maximum capacitance for the Al gate sample in accumulation and a considerable reduction in $Q_{trapped}$ and C-V hysteresis in comparison to the Pt gate sample.

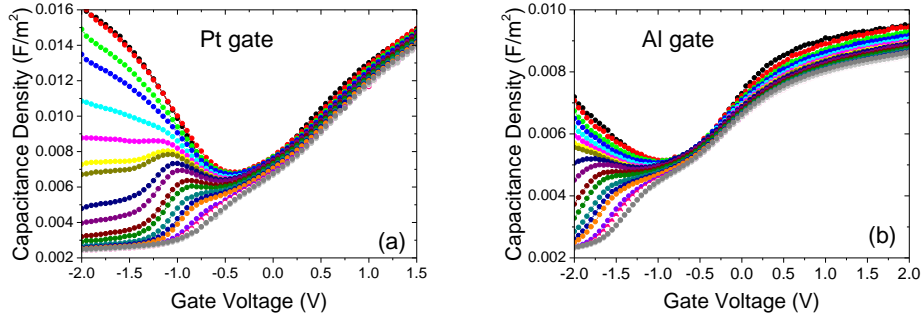


Figure 3.5: Multi-frequency (1kHz to 1MHz) at 295K for (a) Pt/HfO₂(5nm)/n-In_{0.53}Ga_{0.47}As and (b) Al/HfO₂(5nm)/n-In_{0.53}Ga_{0.47}As MOS capacitors.

Further insight into the differences between the Al and Pt gate HfO₂(5nm)/n-In_{0.53}Ga_{0.47}As MOS C-V responses can be obtained from the microstructure of the samples as indicated by TEM images for both samples, as shown in Figures 3.6(a) ~ 3.6(d).

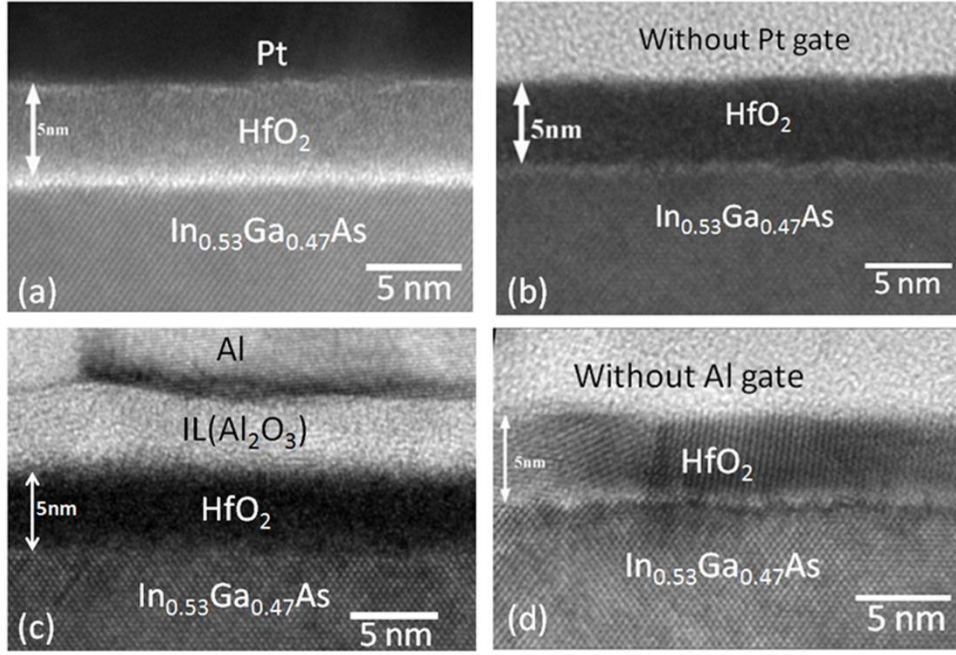


Figure 3.6: TEM micrographs for Pt/HfO₂(5nm)/n-In_{0.53}Ga_{0.47}As MOS capacitor in the area (a) under the Pt gate and (b) outside the Pt gate, and for Al/HfO₂(5nm)/n-In_{0.53}Ga_{0.47}As MOS capacitor in the area (c) under the Al gate and (d) outside the Al gate. Note in (c) the thick interface layer (IL) formed between Al and HfO₂ and the removal of the HfO₂/In_{0.53}Ga_{0.47}As interface oxide.

The Pt gate sample exhibits an interface oxide of 1nm between HfO₂ and the In_{0.53}Ga_{0.47}As. Previous analysis has indicated that this layer is the native oxide of In_{0.53}Ga_{0.47}As and predominantly comprised of a Ga oxide [20]. In Figure 3.4, the maximum capacitance of the Pt gate sample at +1.5V is 0.0146F/m². The oxide capacitance associated with 5nm of HfO₂ ($k=21$) is $C_{ox}=0.037F/m^2$. Even if the Pt gate HfO₂/n-In_{0.53}Ga_{0.47}As MOS sample is driven further into accumulation, it is clear that the experimental capacitance will not acquire the C_{ox} value associated with a 5nm HfO₂ layer alone. This observation also points to a formation of interface oxide with a much lower k -value that is responsible for the reduction in C_{ox} . As observed from Figures 3.6(a) and 3.6(b), this interface oxide layer is present both in the areas under the Pt gate and in the areas outside the Pt gate.

The same interfacial oxide is present for the Al gate sample in the area outside the Al gate (see Figure 3.6(d)). However, the TEM for the Al gate sample taken in the region where the Al gate is present shows that the electron-beam evaporated Al gate results in marked changes in the microstructure of the $\text{HfO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ gate stack. First, a layer of Al_2O_3 of 5nm in thickness is formed between the Al gate and HfO_2 , adding an extra capacitance in series with the total capacitance of the MOS capacitor and thus reducing the maximum capacitance for the Al gate sample, as observed in Figure 3.4. It is noted that a similar Al/ HfO_2 interface layer was also observed in Al/ HfO_2 /Ge MOS structures, as reported in [21]. Second, the presence of the Al gate “scavenges” the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interfacial oxide layer and the $\text{HfO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface oxide is almost gone in the region under the Al gate. This scavenging effect is similar to the effect reported for HfO_2 on silicon MOS structures with a Ti gate [22], but it is noted that for the samples presented in this work (Figure 3.6(c)) the scavenging on the interface oxide layer has occurred during a room temperature Al deposition without any subsequent thermal annealing.

The removal of the native oxide interface layer also has a marked effect on the level of charge trapping, which is estimated from C-V hysteresis at the flat-band capacitance, and is approximately an order of magnitude lower for the Al gate sample than the Pt gate sample even though the Al gate sample is driven further into accumulation. This observation provides strong evidence that the charge trapping responsible for the observed C-V hysteresis is taking place predominantly at the interfacial transition layer between the high- k oxide and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, which can contain native oxides of Ga, In, and As substrate elements [20].

Figure 3.7 illustrates the C-V hysteresis for $\text{Al}_2\text{O}_3(8\text{nm})/n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors using either Ni/Au or Al as metal gates. Due to the reported “self-cleaning” effect of the ALD process to form the Al_2O_3 , reduction of the interfacial oxide between the Al_2O_3 and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ is possible, with improved electrical performance as a result [14, 23-26]. The charge trapping level estimated for $\text{Al}_2\text{O}_3(8\text{nm})/n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors with

reduced $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface layer, using either high (Ni/Au) or low (Al) work function gates is of a level which is around one order of magnitude lower than the typical interface state density in high- $k/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS system.

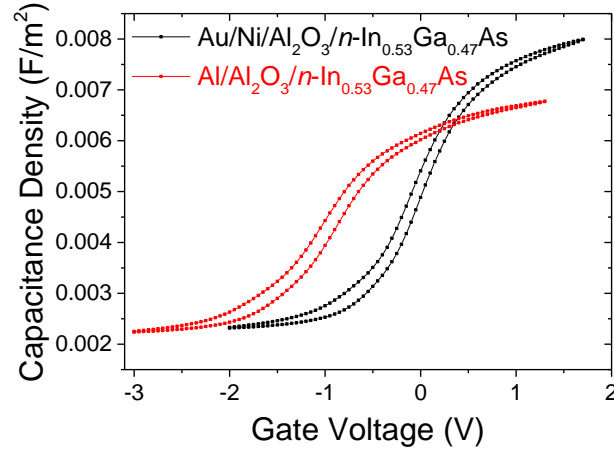


Figure 3.7: C-V hysteresis at 1MHz and 295K for Au/Ni/Al₂O₃(8nm)/n-In_{0.53}Ga_{0.47}As and Al/Al₂O₃(8nm)/n-In_{0.53}Ga_{0.47}As MOS capacitors measured under the same electric field across the Al₂O₃. The charge trapping level of these two samples is relatively low and comparable to the Al/HfO₂/n-In_{0.53}Ga_{0.47}As sample where the interlayer oxide is scavenged by the Al gate. The difference between the two C_{max} values indicates an Al₂O₃ oxide thickness difference of no more than 1.7nm, probably a result of a reactive Al/Al₂O₃ interface compared to a non-reactive Ni/Al₂O₃ interface.

Table 3.2 summaries the charge trapping levels calculated from the C-V hysteresis at flat-band capacitance in Figures 3.4 and 3.7 for the case of samples with different high- $k/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface conditions. This provides further evidence that the charge trapping phenomenon originates from the high- $k/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interfacial transition layer, indicating that engineering of the interface transition region is the key to reducing C-V hysteresis in metal/high- $k/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS systems. In addition, the maximum capacitance for Al/Al₂O₃/In_{0.53}Ga_{0.47}As MOS capacitors is slightly lower than the Au/Ni/Al₂O₃/In_{0.53}Ga_{0.47}As MOS capacitors. This is possibly due to the formation of a thin, self-limiting interface layer of Al₂O₃ between the Al gate and Al₂O₃, which is similar to what is observed in Al/HfO₂/n-

In_{0.53}Ga_{0.47}As MOS structure with a formation of Al₂O₃ between Al and HfO₂. The Al/Al₂O₃ interface layer increases the nominal high-*k* oxide thickness and thus reduces the oxide capacitance, further reducing the total measured capacitance in accumulation (*C*_{max}). As in the case of the C-V in Figure 3.4, the dependence of the capacitance on temperature and ac signal frequency at the bias in nominal accumulation region indicates that genuine surface accumulation has been achieved.

Table 3.2 Summary of charge trapping for the C-V hysteresis shown in Figure 3.4 and Figure 3.7

Sample	<i>Q</i> _{trapped} (cm ⁻²)	High- <i>k</i> / In _{0.53} Ga _{0.47} As interfacial oxide layer	Comments
Pt/HfO ₂ / <i>n</i> -In _{0.53} Ga _{0.47} As	4.7x10 ¹²	Yes	~1nm of HfO ₂ / In _{0.53} Ga _{0.47} As IL
Al/HfO ₂ / <i>n</i> -In _{0.53} Ga _{0.47} As	6.8x10 ¹¹	No	Al scavenges the oxygen from the In _{0.53} Ga _{0.47} As surface
Al/Al ₂ O ₃ / <i>n</i> -In _{0.53} Ga _{0.47} As	8.9x10 ¹¹	No	“Self-cleaning process” of ALD of Al ₂ O ₃ reduces the In _{0.53} Ga _{0.47} As IL
Ni/Al ₂ O ₃ / <i>n</i> -In _{0.53} Ga _{0.47} As	5.9x10 ¹¹	No	“Self-cleaning process” of ALD of Al ₂ O ₃ reduces the In _{0.53} Ga _{0.47} As IL

3.5 Investigating the Distribution of Trapped Charge Based on a High-*k* Thickness Series

Previous experiments and discussions suggest that the border traps are located primarily in the high-*k*/In_{0.53}Ga_{0.47}As interfacial layer. To further examine distribution of the trapped charge, C-V hysteresis was measured as a function of oxide thickness series for Pd/Al₂O₃(5~20nm)/In_{0.53}Ga_{0.47}As (Figure 3.8) [7] and Pd/HfO₂(10~30nm)/In_{0.53}Ga_{0.47}As (Figure 3.9) MOS capacitors. The use of a thickness series is useful in this respect, as for a trapped charge located in a plane within the oxide or at the oxide/semiconductor interface, the C-V hysteresis Δ*V* increases linearly with

increasing oxide thickness. This linear relation can be expressed by the following equation:

$$\Delta V = \frac{q \times Q_{\text{trapped}} \times t_{\text{ox}}}{\epsilon_0 \times k} \quad (3.2)$$

where t_{ox} is the oxide thickness, ϵ_0 is the vacuum permittivity, and k is the relative permittivity of the oxide. If the charge is distributed throughout the oxide, then ΔV is proportional to the square of the oxide thickness [27].

The C-V hysteresis ΔV versus oxide thickness characteristics are shown in Figure 3.8 and Figure 3.9 for Pd/Al₂O₃(5~20nm)/In_{0.53}Ga_{0.47}As and Pd/HfO₂(10~30nm)/In_{0.53}Ga_{0.47}As, respectively. The plots for both oxides clearly demonstrate a linear dependence of ΔV on the oxide thickness for both the *n*- and *p*-type samples, supporting the earlier independent indications in section 3.4 that the vast majority of the charge trapping occurs in a plane (in unit of cm⁻²) near the oxide/semiconductor interface and is not distributed through the oxide (in unit of cm⁻³). The gradient of the plot of ΔV versus the oxide thickness is proportional to the trapped charge and yields values for Al₂O₃ of 2.6x10¹²cm⁻² and 3.6x10¹²cm⁻² for *n*-In_{0.53}Ga_{0.47}As and *p*-In_{0.53}Ga_{0.47}As, respectively, and for HfO₂, of 7.0x10¹²cm⁻² and 8.1x10¹²cm⁻² for *n*-In_{0.53}Ga_{0.47}As and *p*-In_{0.53}Ga_{0.47}As, respectively.

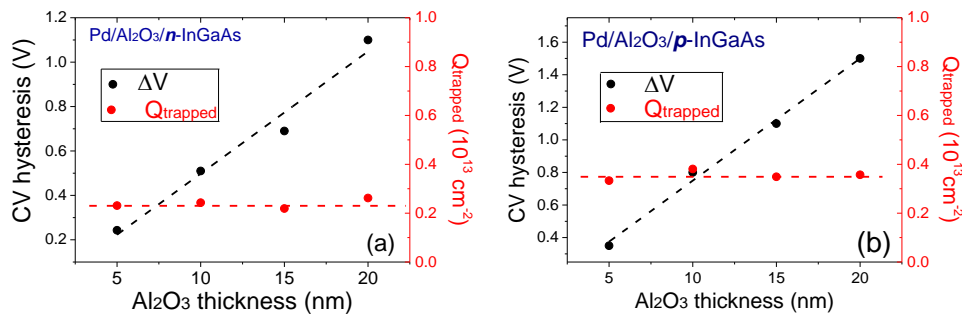


Figure 3.8: C-V hysteresis at 1MHz and 295K as a function of oxide thickness (5, 10, 15, 20nm) for (a) Pd/Al₂O₃/n-In_{0.53}Ga_{0.47}As and (b) Pd/Al₂O₃/p-In_{0.53}Ga_{0.47}As MOS capacitors. The maximum electric field across the oxide, as determined by the maximum voltage in accumulation, is kept at the same value for all thicknesses for both *n*-type and *p*-type sample.

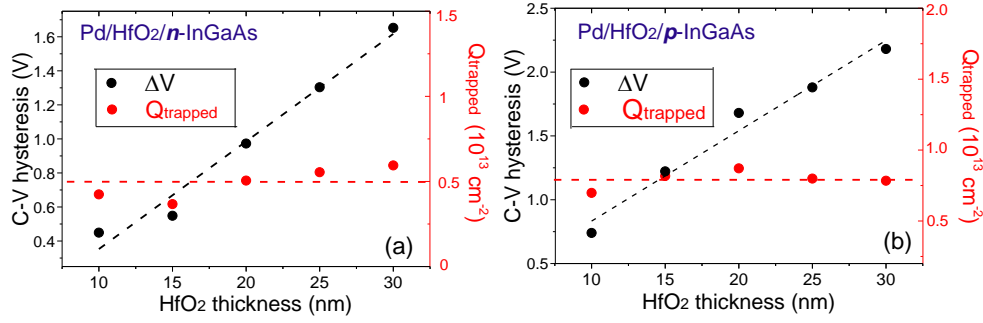


Figure 3.9: C-V hysteresis at 1MHz and 295K as a function of oxide thickness (10, 15, 20, 25, 30nm) for (a) Pd/HfO₂/n-In_{0.53}Ga_{0.47}As and (b) Pd/HfO₂/p-In_{0.53}Ga_{0.47}As MOS capacitors. The maximum electric field across the oxide, as determined by the maximum voltage in accumulation, is kept at the same value for all thicknesses for both n-type and p-type sample.

3.6 Conclusions

In this chapter, charge trapping behavior in metal/high-*k*/In_{0.53}Ga_{0.47}As/InP MOS structures with either HfO₂ or Al₂O₃ ALD deposited high-*k* oxides was studied using C-V hysteresis measurements in combination with TEM microscopy analysis. The samples studied employed both high work function metal gates (Pt, Pd, Ni/Au) and a low work function metal gate (Al). The high-*k*/In_{0.53}Ga_{0.47}As MOS system exhibits both electron and hole trapping, which is predominantly a reversible process. The charge trapping levels, that can be as high as 10¹³cm⁻², were recorded from the C-V hysteresis which is of the same magnitude as, or even greater than the high-*k*/In_{0.53}Ga_{0.47}As interface state density, indicating the importance of C-V hysteresis in the high-*k*/In_{0.53}Ga_{0.47}As MOS system. As the border traps are located in the high-*k*/In_{0.53}Ga_{0.47}As interface layer, which extends approximately 1nm into the high-*k* oxide, the surface density of 10¹³cm⁻² corresponds to a volume density of 10²⁰cm⁻³. C-V hysteresis is found to increase with the increasing bias in accumulation, and the *p*-type In_{0.53}Ga_{0.47}As MOS samples exhibit a larger C-V hysteresis and permanent charge trapping than their *n*-type In_{0.53}Ga_{0.47}As counterparts.

Based on TEM analysis, it is observed that the use of an Al gate in HfO₂/In_{0.53}Ga_{0.47}As samples results in the formation of an Al₂O₃ layer at the

top Al/high- k oxide interface which reduces the maximum capacitance in accumulation. In addition, the top Al metal layer reduces the thickness of the native oxide transition layer present between the HfO_2 and the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ surface. The removal of the native oxide transition layer for the Al gate samples results in a marked reduction in the level of charge trapping and C-V hysteresis when compared to a Pt gate $\text{HfO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ sample with $\sim 1\text{nm}$ of $\text{HfO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface oxide, indicating that the charge trapping takes place mainly at the interfacial transition layer between the high- k oxide and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$. In addition, $\text{Al}/\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and $\text{Au}/\text{Ni}/\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors, which have reduced interface oxide due to the reported “self-cleaning” effect of Al_2O_3 by ALD, have a relatively low level of charge trapping.

The C-V hysteresis voltage window (ΔV) is found to increase linearly with the increasing high- k oxide thickness, with the corresponding trapped charge being independent of the oxide thickness for both Al_2O_3 and HfO_2 , providing further evidence that the trapped charge is predominantly localized as a line charge (in units in cm^{-2}) at or near the high- $k/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface. The results presented in this work identify the understanding and engineering of a native oxide interfacial transition layer between the high- k oxide and the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ surface, as central to reducing C-V hysteresis in the high- $k/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS systems.

Bibliography

- [1] Y. Yuan, L. Wang, B. Yu, B. Shin, J. Ahn, P. C. McIntyre, P. M. Asbeck, M. J. W. Rodwell, and Y. Taur, *IEEE Electron Device Lett.* **32**(4), 485–487 (2011).
- [2] G. Brammertz, A. Alian, D. H. C. Lin, M. Meuris, M. Caymax, and W.-E. Wang, *IEEE Trans. Electron Devices* **58**(11), 3890–3897 (2011).
- [3] E. J. Kim, L. Wang, P. M. Asbeck, K. C. Saraswat, and P. C. McIntyre, *Appl. Phys. Lett.* **96**, 012906 (2010).
- [4] A. Alian, G. Brammertz, R. Degraeve, M. Cho, C. Merckling, D. Lin, W.-E. Wang, M. Caymax, M. Meuris, K. D. Meyer, and M. Heyns, *IEEE Electron Device Lett.* **33**(11), 1544–1546 (2012).
- [5] G. Brammertz, H. C. Lin, M. Caymax, M. Meuris, M. Heyns, and M. Passlack, *Appl. Phys. Lett.* **95**, 202109 (2009).
- [6] N. Taoka, M. Yokoyama, S. H. Kim, R. Suzuki, R. Iida, S. Lee, T. Hoshii, W. Jevasuwan, T. Maeda, T. Yasuda, O. Ichikawa, N. Fukuhara, M. Hata, M. Takenaka, and S. Takagi, in *Proceedings of the IEEE International Electron Devices Meeting—IEDM (IEEE, 2011)*, p. 610.
- [7] Y. Y. Gomeniuk, A. N. Nazarov, S. Monaghan, K. Cherkaoui, E. O'Connor, I. Povey, V. Djara, and P. K. Hurley, in *Proceedings of the International Conference on nanomaterials: Applications and Properties* (2012), vol. **1**, no. 3, p. 03TF16.
- [8] N. Goel, D. Heh, S. Koveshnikov, I. Ok, S. Oktyabrsky, V. Tokranov, R. Kambhampati, M. Yakimov, Y. Sun, P. Pianetta, C. K. Gaspe, M. B. Santos, J. Lee, S. Datta, P. Majhi, and W. Tsai, *Tech. Dig. - Int. Electron Devices Meet.* 363–366 (2008).
- [9] E. O'Connor, B. Brennan, V. Djara, K. Cherkaoui, S. Monaghan, S. B. Newcomb, R. Contreras, M. Milojevic, G. Hughes, M. E. Pemble, R. M. Wallace, and P. K. Hurley, *J. Appl. Phys.* **109**, 024101 (2011).
- [10] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices* (Wiley, NJ, 2007).
- [11] E. H. Nicollian and J. R. Brews, *MOS Physics and Technology* (Wiley, New York, 2003).

- [12] K. Cherkaoui, S. Monaghan, M. A. Negara, M. Modreanu, P. K. Hurley, D. O’Connell, S. McDonnell, G. Hughes, S. Wright, R. C. Barklie, P. Bailey, and T. C. Q. Noakes, *J. Appl. Phys.* **104**, 064113 (2008).
- [13] D. P. Norton, *Mater. Sci. Eng. R* **43**, 139–247 (2004).
- [14] A. O’Mahony, S. Monaghan, G. Provenzano, I. M. Povey, M. G. Nolan, E. O’Connor, K. Cherkaoui, S. B. Newcomb, F. Crupi, P. K. Hurley, and M. E. Pemble, *Appl. Phys. Lett.* **97**, 052904 (2010).
- [15] R. D. Long, B. Shin, S. Monaghan, K. Cherkaoui, J. Cagnon, S. Stemmer, P. C. McIntyre, and P. K. Hurley, *J. Electrochem. Soc.* **158**, G103 (2011).
- [16] T. S. Böske, J. Müller, D. Bräuhäus, U. Schröder, and U. Böttger, *Appl. Phys. Lett.* **99**, 102903 (2011).
- [17] J. Müller, T. S. Böske, D. Bräuhäus, U. Schröder, U. Böttger, J. Sundqvist, P. Kücher, T. Mikolajick, and L. Frey, *Appl. Phys. Lett.* **99**, 112901 (2011).
- [18] M. Kobayashi, P. T. Chen, Y. Sun, N. Goel, P. Majhi, M. Garner, W. Tasai, P. Pianetta, and Y. Nishi, *Appl. Phys. Lett.* **93**, 182103 (2008).
- [19] P. K. Hurley, E. O’Connor, S. Monaghan, R. D. Long, A. O’Mahony, I. M. Povey, K. Cherkaoui, J. MacHale, A. J. Quinn, G. Brammertz, M. Heyns, S. B. Newcomb, V. V. Afanas’ev, A. M. Sonnet, R. V. Galatage, M. N. Jivani, E. M. Vogel, R. M. Wallace and M. E. Pemble, *ECS Trans.* **25**(6), 113 (2009).
- [20] R. D. Long, E. O’Connor, S. B. Newcomb, S. Monaghan, K. Cherkaoui, P. Casey, G. Hughes, K. K. Thomas, F. Chalvet, I. M. Povey, M. E. Pemble, and P. K. Hurley, *J. Appl. Phys.* **106**, 084508 (2009).
- [21] S. Rangan, E. Bersch, R. A. Bartynski, E. Garfunkel, and E. Vescovo, *Appl. Phys. Lett.* **92**, 172906 (2008).
- [22] H. Kim, P. C. McIntyre, C. O. Chui, K. C. Saraswat, and S. Stemmer, *J. Appl. Phys.* **96**, 3467 (2004).
- [23] S. Klejna and S. D. Elliot, *J. Phys. Chem. C* **116**(1), 643–654 (2012).
- [24] E. J. Kim, E. Chagarov, J. Cagnon, Y. Yuan, A. C. Kummel, P. M. Asbeck, S. Stemmer, K. C. Saraswat, and P. C. McIntyre, *J. Appl. Phys.* **106**, 124508 (2009).

- [25] M. Milojevic, F. S. Aguirre-Tostado, C. L. Hinkle, H. C. Kim, E. M. Vogel, J. Kim, and R. M. Wallace, *Appl. Phys. Lett.* **93**, 202902 (2008).
- [26] S. Monaghan, A. O'Mahony, G. Provenzano, K. Cherkaoui, E. O'Connor, I. M. Povey, M. G. Nolan, D. O'Connell, S. B. Newcomb, F. Crupi, M. E. Pemble, and P. K. Hurley, *J. Vac. Sci. Technol. B* **29**(1), 01A807 (2011).
- [27] R. S. Muller and T. I. Kamins, *Device Electronics for Integrated Circuits* (Wiley, New York, 1986).

Chapter 4: Dynamics of Charge Trapping in High- $k/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS Capacitors

4.1 Introduction

In this chapter, the work in chapter 3 is extended to study C-V hysteresis in $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and $\text{HfO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors with an emphasis on a study of the charge trapping dynamics through analysis of the C-V hysteresis evolution with the hold time in accumulation, which provides further insight into the charge trapping behavior in the high- $k/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS system. Section 4.2 will detail the experiments. Analysis of C-V hysteresis performed with a hold time in accumulation will be discussed in section 4.3. A study of charge trapping relaxation will be presented in section 4.4, and section 4.5 will conclude the whole chapter.

4.2 Experimental Details

The samples used in this work were n -doped and p -doped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ (doping level is $4 \times 10^{17} \text{cm}^{-3}$) epitaxial layers ($2 \mu\text{m}$), respectively, grown by metal organic vapour phase epitaxy (MOVPE). Details of the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ have been given in chapter 2 section 2.5. Prior to oxide deposition, all the samples were immersed in $(\text{NH}_4)_2\text{S}$ solutions (10% in deionized H_2O) for 20min at room temperature ($\sim 295\text{K}$) [1]. The samples were then introduced to the atomic layer deposition (ALD) chamber within a minimum transfer time ($\sim 3\text{min}$) after the removal from the 10% $(\text{NH}_4)_2\text{S}$ solution. Either HfO_2 or Al_2O_3 was deposited as the high- k oxide on the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ surface. The HfO_2 dielectric has a nominal thickness of 15nm deposited by ALD at 250°C

using $\text{Hf}[\text{N}(\text{CH}_3)\text{C}_2\text{H}_5]_4$ (TEMAH) and H_2O as precursors. The Al_2O_3 dielectric has a nominal thickness of 8nm deposited by ALD at 300°C using trimethylaluminum (TMA) $\text{Al}(\text{CH}_3)_3$ and H_2O as precursors. Pd(160nm) was used as the metal contacts for the HfO_2 on $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS structure. Al(160nm) was used as the metal gate for the $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ structure. Pd and Al gates were formed by electron beam evaporation and a lift-off process. Table 4.1 gives the sample details used in this chapter. The measurements discussed in this chapter were recorded using an E4980 LCR meter controlled through labview which is capable of measuring C-V from inversion to accumulation at a gate voltage (V_g) equals to V_{max} and holding MOS capacitor at V_{max} for a period of hold time (or stress time, t_{stress}) before sweeping the C-V back towards inversion.

Table 4.1 Sample details: SP stands for Surface Preparation in 10% $(\text{NH}_4)_2\text{S}$ solution

Sample	Oxide	Gate metal	SP
$\text{Al}_2\text{O}_3/n\text{-} \& p\text{-} \text{In}_{0.53}\text{Ga}_{0.47}\text{As}$	$\text{Al}_2\text{O}_3(8\text{nm})$	Al (160nm)	Yes
$\text{HfO}_2/n\text{-} \& p\text{-} \text{In}_{0.53}\text{Ga}_{0.47}\text{As}$	$\text{HfO}_2(15\text{nm})$	Pd (160nm)	Yes

4.3 C-V Hysteresis as a Function of Stress Time

4.3 a) $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS Structures

C-V hysteresis with a hold in accumulation (at V_{max}) will be discussed in this section. Figure 4.1 shows the C-V hysteresis responses with an increasing stress time in accumulation (at V_{max}) for the Al gate $\text{Al}_2\text{O}_3(8\text{nm})$ sample over (a) $n\text{-}\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and (b) $p\text{-}\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors. The values of V_{max} were chosen to be a gate voltage at which the gate current is measured above the noise level and in the meantime much smaller than the breakdown voltage in order to avoid breakdown during the stress.

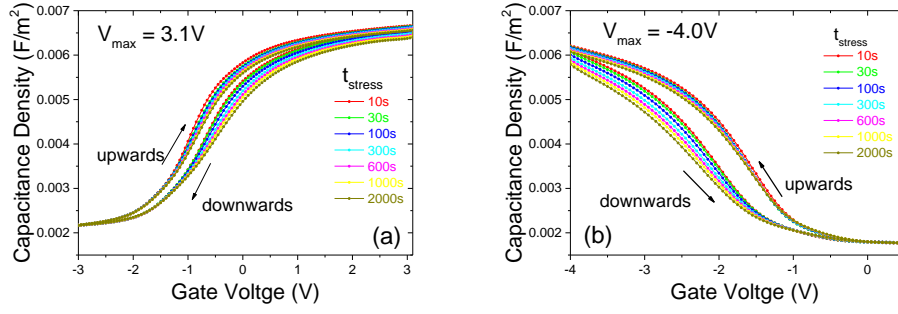


Figure 4.1: C-V hysteresis responses measured at 1MHz and 295K with an increasing stress time in accumulation at V_{max} for (a) Al/Al₂O₃(8nm)/n-In_{0.53}Ga_{0.47}As and (b) Al/Al₂O₃(8nm)/p-In_{0.53}Ga_{0.47}As MOS capacitors.

The C-V hysteresis extracted from Figure 4.1 is plotted as a function of stress time and is shown in Figure 4.2. Figure 4.2 indicate the C-V hysteresis increases with a power law dependence on the increasing stress time at V_{max} , consistent with the model by S. Zafar *et al* [2] for stress times that are not long. It is important to emphasize that $\Delta V \neq 0V$ even without a stress time at V_{max} . This ΔV value at a stress time of 0 seconds ($t_{stress}=0$) is denoted as ΔV_0 . ΔV_0 is small for Al₂O₃/In_{0.53}Ga_{0.47}As MOS structure so can be neglected. However, in future work ΔV_0 should be considered for more accurate model establishment as in the case for HfO₂/In_{0.53}Ga_{0.47}As MOS structure which will be discussed later.

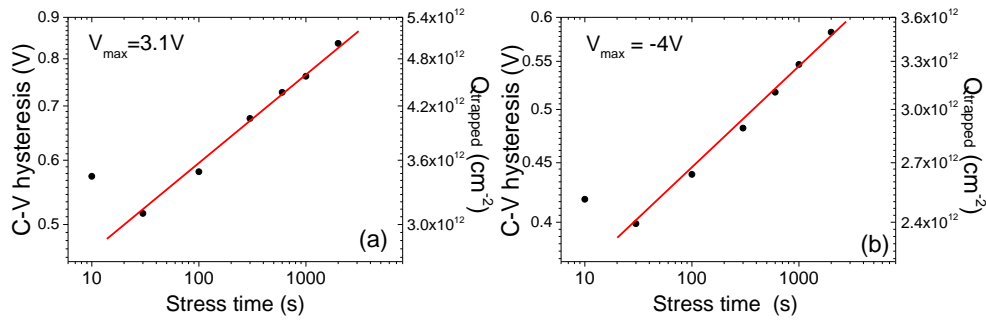


Figure 4.2: C-V hysteresis as a function of stress time in accumulation at V_{max} for (a) Al/Al₂O₃(8nm)/n-In_{0.53}Ga_{0.47}As and (b) Al/Al₂O₃(8nm)/p-In_{0.53}Ga_{0.47}As MOS capacitors. Note that C-V hysteresis (and $Q_{trapped}$) versus stress time is plotted in a log-log scale.

It is also observed in Figure 4.2 that the ΔV at $t_{\text{stress}}=10\text{s}$ is larger than that at $t_{\text{stress}}=30\text{s}$, and this is due to the permanent charge trapping associated C-V shift which appears the most noticeable when measured on a fresh device [3]. Note that the C-V hysteresis sweeps with increasing stress times are measured on the same site for both n - and p -type $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ samples.

In order to investigate the relation between the trapped charge (Q_{trapped}) and the injected charge (Q_{injected}), gate current was measured as a function of the stress time at V_{max} . An example is shown in Figure 4.3. Taking the integration of the gate current density (cm^{-2}) over the stress time (red shadow area in Figure 4.3) gives the total charge injected (cm^{-2}) through the oxide during the stress at V_{max} . This measurement was performed on a variety of sites and the injected charge density values over these sites were averaged in order that the presented Q_{injected} values in this study are representative of the sample behavior.

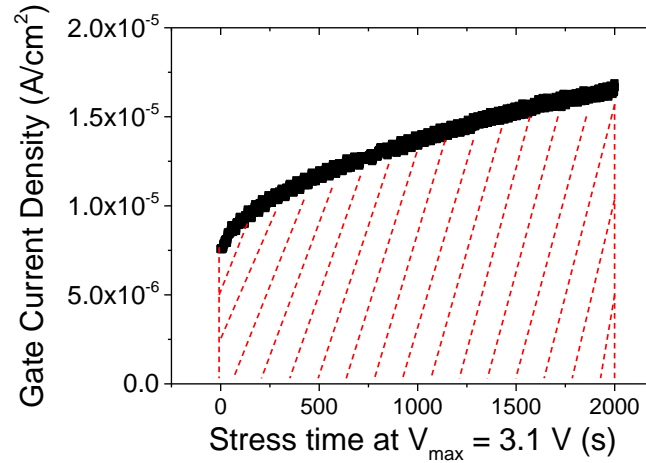


Figure 4.3: Gate current density as a function of stress time for an $\text{Al}/\text{Al}_2\text{O}_3(8\text{nm})/n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitor measured at $V_g = V_{\text{max}} = 3.1\text{V}$.

Charge trapping efficiency (η_{trapping}) is defined as the ratio of the trapped charge density to the injected charge density (see equation (4.1)).

$$\eta_{\text{trapping}} = \frac{Q_{\text{trapped}}}{Q_{\text{injected}}} \times 100\% \quad (4.1)$$

Charge trapping efficiency is plotted as a function of Q_{injected} in Figure 4.4 for the Al gate $\text{Al}_2\text{O}_3(8\text{nm})$ over (a) $n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ and (b) $p\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors. It is observed that η_{trapping} decreases with a power law dependence on the increasing Q_{injected} , as predicted from the ΔV_T versus Q_{injected} model by S. Zafar *et al* [2] (see Appendix IV).

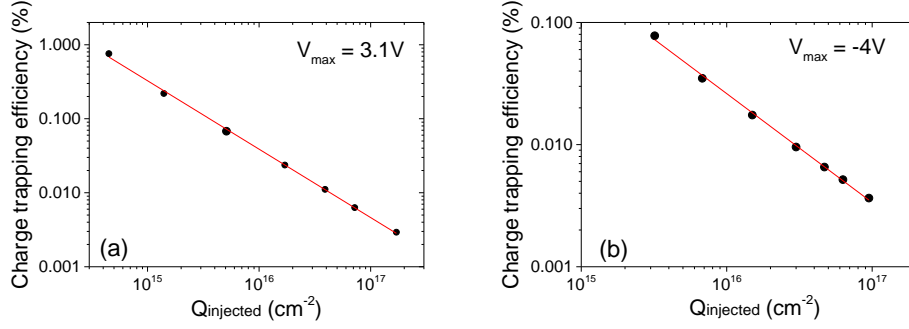


Figure 4.4: Charge trapping efficiency as a function of injected charge density for (a) $\text{Al}/\text{Al}_2\text{O}_3(8\text{nm})/n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ and (b) $\text{Al}/\text{Al}_2\text{O}_3(8\text{nm})/p\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors.

4.3 b) $\text{HfO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS Structures

For the $\text{HfO}_2(15\text{nm})/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS structures, the gate current during stress was affected by noise due to the large amount of defect sites in HfO_2 film that contribute to the conduction/leakage, and as a result it was not possible for these structures to obtain reliable values for the charge injected. As a consequence of the current noise, a different approach was used to analyze the charge trapping dynamics for the $\text{HfO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors based on an analysis of the time evolution of the measured C-V hysteresis ΔV values.

For $\text{HfO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS systems which have a large portion of permanent charge trapping component, measurements with different stress times were performed on different sites in order to rule out the contribution of the permanent charge trapping associated C-V shift [3], and in the meantime, to minimize the possible contribution of stress induced defects to the measured value of ΔV . The behavior of these sites has been confirmed to be similar by comparing the double C-V hysteresis measured on them prior

to the stress measurements. In addition, a thicker oxide, HfO_2 of 15nm, was chosen in order that the capacitor could sustain after a stress time up to 100,000s, without experiencing irreversible electrical breakdown.

Figure 4.5 and Figure 4.6 show the evolution of the C-V hysteresis with increasing stress time (0s to 100ks) in accumulation for Pd gate/ HfO_2 (15nm) over $n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ and $p\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors with different values of V_{max} .

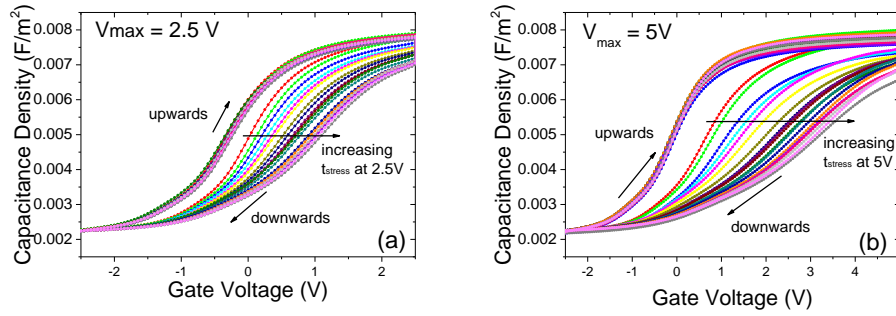


Figure 4.5: C-V hysteresis responses with an increasing stress time (0s to 100ks) in accumulation for (a) Pd/ HfO_2 (15nm)/ $n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ ($V_{\text{max}}=2.5\text{V}$), (b) Pd/ HfO_2 (15nm)/ $n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ ($V_{\text{max}}=5\text{V}$). Note that the red curve is C-V hysteresis with no hold time at V_{max} .

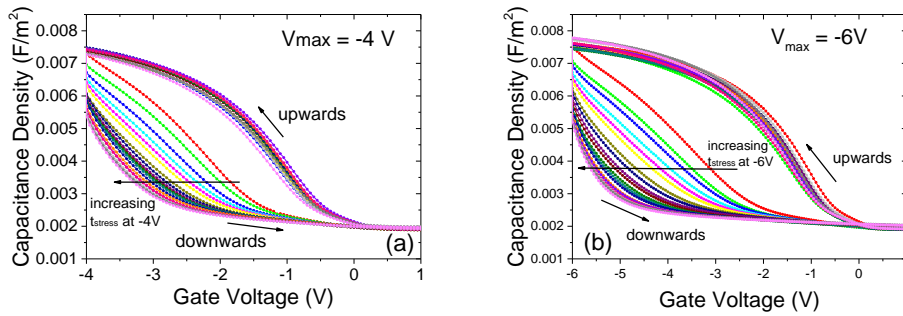


Figure 4.6: C-V hysteresis responses with an increasing stress time (0s to 100ks) in accumulation for (a) Pd/ HfO_2 (15nm)/ $p\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ ($V_{\text{max}}=-4\text{V}$), and (b) Pd/ HfO_2 (15nm)/ $p\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ ($V_{\text{max}}=-6\text{V}$). Note that the red curve is C-V hysteresis with no hold time at V_{max} .

It is evident from both the n - and p -type HfO_2 MOS samples that the C-V responses on the downward sweep is not parallel shifted with respect to the

upward sweep. This is also the case for the Al_2O_3 MOS samples in Figure 4.1, however, the effect is not as prominent for the $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ structures. The change of slope for the downward C-V response is indicative of the release of trapped charge during the C-V sweep, and as a consequence, the C-V response is not unique, and will depend on the time associated with the measurement. These results imply that, if the C-V measurements could be performed in a shorter time period, a larger C-V hysteresis (and an associated higher trapped charge density) would be recorded. This effect can be investigated by the stress-relaxation measurement, and is covered in section 4.4.

It is noted that ΔV_0 (see the red curve in Figure 4.5 and 4.6) is not negligible in the case of HfO_2 , therefore ΔV_0 must be taken into account when considering the ΔV versus t_{stress} model. $\Delta V - \Delta V_0$ is plotted as a function of stress time for $\text{HfO}_2(15\text{nm})$ over (a) $n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ and (b) $p\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors using different values of V_{max} as shown in Figure 4.7 in log-log scale. It is observed that $\Delta V - \Delta V_0$ increases with a power law dependence with the increasing stress time at the initial stage of stressing and tends to reach a plateau when the stress time is sufficiently long [4]. This relation is similar to the previous model proposed by S. Zafar *et al* [2], who performed positive bias stress pulses on HfO_2 and Al_2O_3 on Si substrate n -channel MOSFET and demonstrated that the threshold voltage shift (ΔV_T) increases with a power law dependence on the stress time at the initial stage of stressing. This model also predicts that the ΔV_T will eventually reach a plateau if the n -channel MOSFET is stressed at positive gate bias for a sufficiently long time providing that no new border traps are created during the stress. The relation between $\Delta V - \Delta V_0$ and stress time (t_{stress}) can be expressed using equation (4.2) on the premise that no new traps are generated during the stress.

$$\Delta V - \Delta V_0 = \Delta V_{\text{max}0} \times \{1 - \exp(-(\frac{t_{\text{stress}}}{\tau_0})^\gamma)\} \quad (4.2)$$

where τ_0 and γ are fitting parameters associated with the gate leakage current and the capture cross section of the traps, and $\Delta V_{\text{max}0}$ is associated with the maximum trapping density [2]. For $t_{\text{stress}} \ll \tau_0$, $\Delta V - \Delta V_0 \approx \Delta V_{\text{max}0} \times (t_{\text{stress}}/\tau_0)^\gamma$

(i.e. a power law dependence of $\Delta V - \Delta V_0$ on t_{stress}), and for $t_{\text{stress}} \gg \tau_0$, $\Delta V - \Delta V_0 \approx \Delta V_{\text{max}0}$ (i.e. a plateau). The observed plateau at sufficiently long stress times indicates the filling of almost all the border trap energy levels is achieved under a certain value of V_{max} or oxide field (E_{ox}). Once $\Delta V_{\text{max}0}$ is obtained (i.e. the saturation value of $\Delta V - \Delta V_0$ in Figure 4.7), the maximum trapping density corresponding to a certain value of V_{max} used, can be calculated using equations (4.2). The values are included in the Table 4.2.

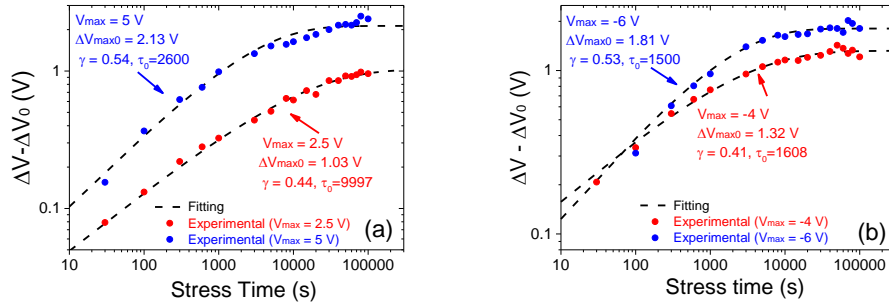


Figure 4.7: $\Delta V - \Delta V_0$ as a function of stress time for (a) $\text{Pd}/\text{HfO}_2(15\text{nm})/\text{n-In}_{0.53}\text{Ga}_{0.47}\text{As}$ and (b) $\text{Pd}/\text{HfO}_2(15\text{nm})/\text{p-In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors. $\Delta V - \Delta V_0$ increases with a power law dependence with the increasing t_{stress} at the initial stage of stressing and tends to reach a plateau at sufficiently long stress times.

Table 4.2 Summary of fitting parameters for stressing measurements for $\text{HfO}_2(15\text{nm})/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ shown in Figure 4.7

Sample	V_{max}	$\Delta V_{\text{max}0}$	max. Q_{trapped}	τ_0	γ
$\text{n-In}_{0.53}\text{Ga}_{0.47}\text{As}$	2.5V	1.03V	$9.2 \times 10^{12} \text{cm}^{-2}$	9997	0.44
$\text{n-In}_{0.53}\text{Ga}_{0.47}\text{As}$	5V	2.13V	$2.0 \times 10^{13} \text{cm}^{-2}$	2600	0.54
$\text{p-In}_{0.53}\text{Ga}_{0.47}\text{As}$	-4V	1.32V	$1.6 \times 10^{13} \text{cm}^{-2}$	1608	0.41
$\text{p-In}_{0.53}\text{Ga}_{0.47}\text{As}$	-6V	1.81V	$2.7 \times 10^{13} \text{cm}^{-2}$	1500	0.53

It is noted in Figure 4.7 and Table 4.2 that using different V_{max} results in different saturation values at the plateau. Border traps can be distributed at different energy levels and also at different depth into the oxide near/at the

high- k /In_{0.53}Ga_{0.47}As interface (Figure 4.8) [5-7]. Firstly, using a larger V_{\max} pushes the Fermi level further into the In_{0.53}Ga_{0.47}As conduction/valence bands during the stress time at V_{\max} , thus accessing border traps over a wider energy range resulting in a larger C-V hysteresis. Secondly, a larger V_{\max} increases the electric field across the oxide (E_{ox}), which can result in additional oxide traps being aligned with the Fermi level at the high- k /In_{0.53}Ga_{0.47}As interface during the stress (see Figure 4.8), and consequently being available for interaction via a tunnelling process.

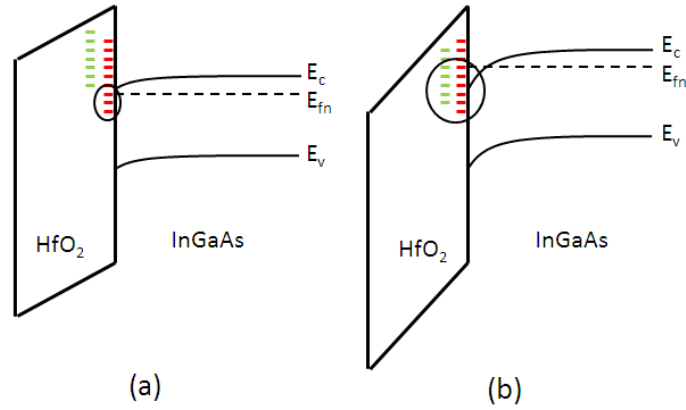


Figure 4.8: Simplified band diagrams of HfO₂/n-In_{0.53}Ga_{0.47}As MOS capacitor which have (a) smaller V_{\max} (or E_{ox}) and (b) larger V_{\max} (or E_{ox}). The border traps that are involved in the trapping process leading to C-V hysteresis are circled. Using a larger V_{\max} thus a larger E_{ox} allows more border traps to be accessed, resulting in a larger maximum C-V hysteresis and charge trapping.

4.4 Study of Charge Trapping Relaxation in HfO₂/In_{0.53}Ga_{0.47}As MOS structures

It is noted that for most of the measured C-V hysteresis on high- k /In_{0.53}Ga_{0.47}As MOS structures, the C-V hysteresis is not an exact parallel loop, as illustrated in an example in Figure 4.9 where the experimental downward C-V sweep is not perfectly parallel to the upward C-V. This is because a portion of trapped charges (electrons in Figure 4.9) are being removed (or de-trapped) from the trapping sites during the downward C-V where the Fermi level is pushed away from the conduction band edge even

before reaching the flatband condition. This results in an underestimation of Q_{trapped} from standard C-V hysteresis tests, therefore a study of charge de-trapping (or charge trapping relaxation) is necessary.

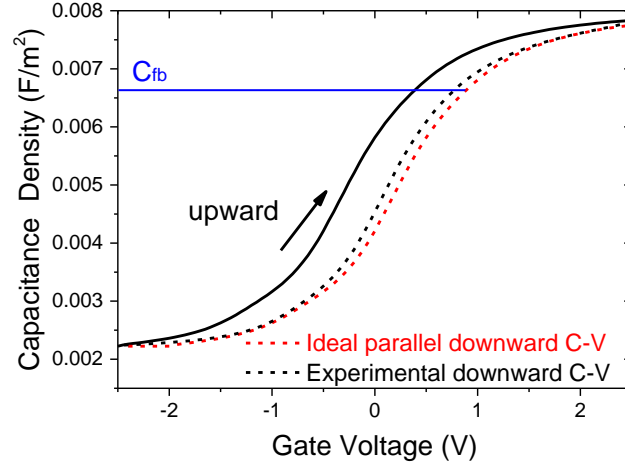


Figure 4.9: C-V hysteresis loop for Pd/HfO₂(15nm)/n-In_{0.53}Ga_{0.47}As MOS structure. The measured C-V hysteresis loop is not a perfect parallel shift due to charge de-trapping (or charge trapping relaxation). Note that the ideal parallel downward C-V (in red) is drawn for illustrative purpose only.

To account for charge trapping relaxation, a set of measurement with both stress phase and relaxation phase was performed on HfO₂/In_{0.53}Ga_{0.47}As MOS capacitors. The stress-relaxation scheme is illustrated in Figure 4.10, during both phases capacitance was measured as a function of time. Prior to the stress-relaxation measurement, a C-V sweep was firstly measured on a fresh device to estimate the V_{fb} , where V_{fb} was taken as the voltage at which the maximum C-V slope occurred [8]. On another fresh device, a C-V characteristic with a much smaller bias range around the estimated V_{fb} was carried out, and V_{fb} was estimated again from the small bias range C-V response. These measurements assured that a more accurate V_{fb} value (V_{fb0}) was obtained from a less stretched-out C-V. On the same device, a stress voltage ($V_g = V_{\text{stress}} = V_{\text{ov}} + V_{\text{fb0}}$, where V_{ov} is the overdrive voltage) beyond the V_{fb0} value into accumulation was applied for a series of stress time (t_{stress}). After each t_{stress} , the applied voltage was set back to $V_g = V_{\text{relax}} = V_{\text{fb0}}$ for relaxation time ($t_{\text{relax}} \approx 4\text{s}$) in order to account for the relaxation due to de-trapping of charge trapped at the stress voltage.

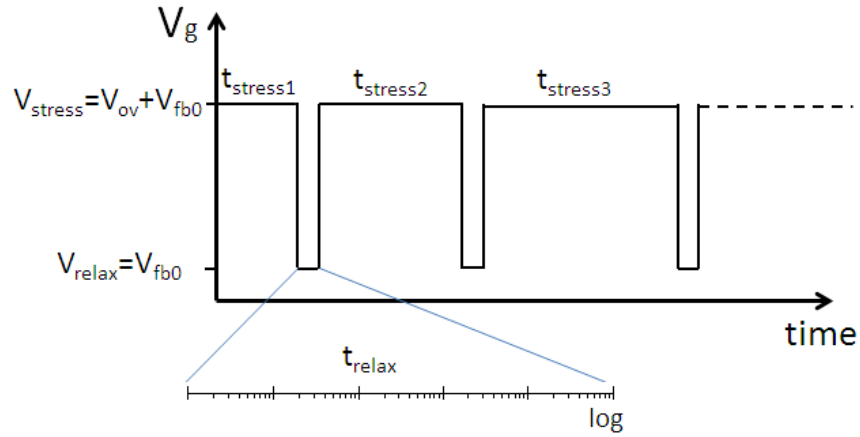


Figure 4.10: Sketches of the stress-relaxation measurements. During both stress phase and relaxation phase, capacitance was measured as a function of time. During the relaxation phase, capacitance was measured at a sampling rate which covered logarithmic time scale.

An example of capacitance as a function of time is illustrated in Figure 4.11 for Pd/HfO₂(15nm)/n-In_{0.53}Ga_{0.47}As MOS capacitor and $V_{\text{ov}}=1.2\text{V}$ was used during the stress phase. During the stress phase, the capacitance is decreasing with the increasing stress time, consistent with C-V progressively shifting positively along the gate voltage axis due to more charges (electrons) being trapped with increasing t_{stress} . When the measurement is switched from stress phase (at $V_{\text{ov}} + V_{\text{fb0}}$) to relaxation phase (at V_{fb0}), there is a very large drop in capacitance (from $\sim 3.75 \times 10^{11}\text{F}$ down to $\sim 2.05 \times 10^{11}\text{F}$), and during the relaxation phase, the capacitance increases as a function of t_{relax} and this results from the C-V shifting negatively towards the initial C-V before the stress due to the electron de-trapping (or V_{fb} shift recovery). Finally, a C-V response with a full bias range was measured on the device in order to check the device was not broken down after the stress measurements.

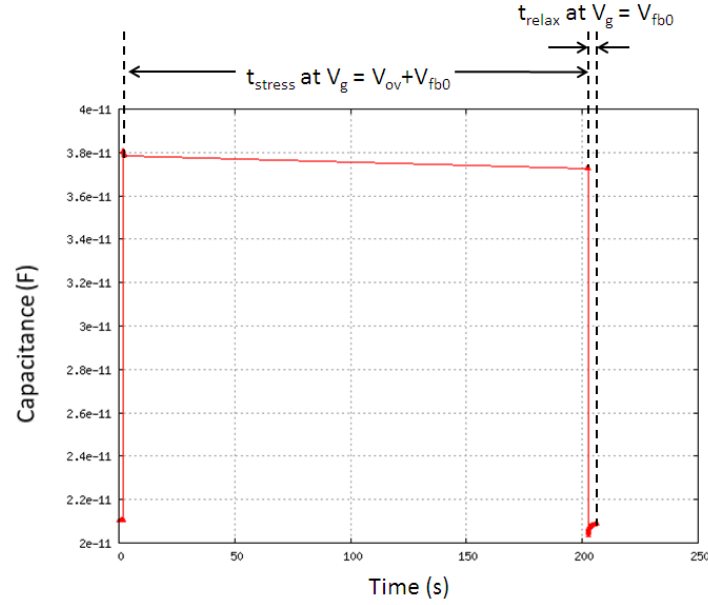


Figure 4.11: Capacitance as a function of time during the stress phase ($V_{ov}=1.2V$) and the relaxation phase for $Pd/HfO_2(15nm)/n-In_{0.53}Ga_{0.47}As$ MOS capacitor.

Figure 4.12 shows the flatband voltage shift (ΔV_{fb}) as a function of relaxation time (t_{relax}) in the relaxation phase (at $V_g=V_{fb0}$) after stress measurements ($V_{ov}=1.2V$) for a series of stress time (t_{stress}) for $Pd/HfO_2(15nm)/n-In_{0.53}Ga_{0.47}As$ MOS structure. It is observed that for each stress time, ΔV_{fb} is decreasing towards zero during the relaxation phase ($\sim 4s$), indicating that the trapped electrons are being removed or “recovered” from the trapping sites during the relaxation phase. Similar results have been observed in $HfO_2/p-In_{0.53}Ga_{0.47}As$ MOS structures (not shown). These results are consistent with the significant threshold voltage shift (ΔV_{th}) recovery during relaxation phase observed in $Al_2O_3/n-In_{0.53}Ga_{0.47}As$ high-electron mobility transistors (HEMT) as reported in [9]. It is noted that the relaxation process for trapped charges in the $In_{0.53}Ga_{0.47}As$ MOS structure is much faster when compared to metal gate/high- k /silicon based MOS devices (see Figure 4.13). As a consequence of this fast relaxation process, due to de-trapping of electrons, the trapped charge associated with C-V hysteresis at 1MHz is an underestimation of the full trapped charge, as the time associated with a full C-V sweep at 1 MHz is typically in the range of 10’s of seconds.

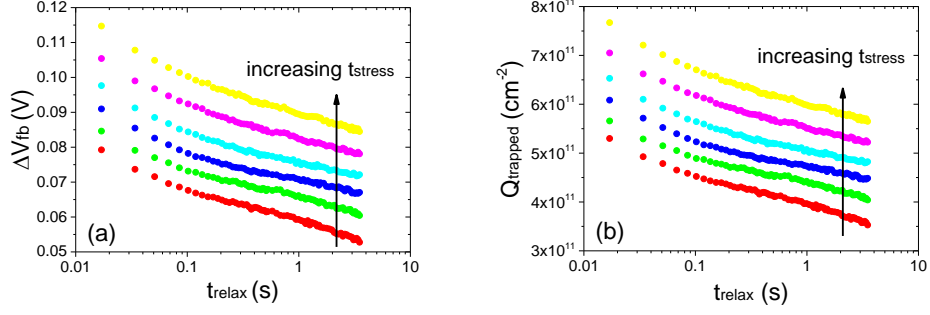


Figure 4.12: (a) Flatband voltage shift (ΔV_{fb}) as a function of relaxation time (t_{relax}) and (b) the corresponding charge trapping density ($Q_{trapped}$) in the relaxation phase (at $V_g = V_{fb0}$) after stress measurements ($V_{ov} = 1.2V$) for a series of stress time (t_{stress}) for $Pd/HfO_2(15nm)/n-In_{0.53}Ga_{0.47}As$ MOS capacitor.

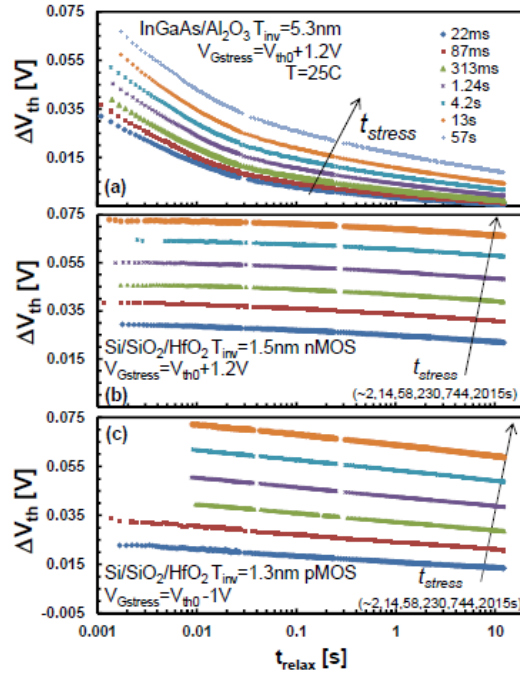


Figure 4.13: Threshold voltage shift (ΔV_{th}) as a function of relaxation time (t_{relax}) for (a) $Al_2O_3/n-In_{0.53}Ga_{0.47}As$, (b) high-k/Si n-MOS and (b) high-k/Si p-MOS devices, showing that the relaxation process is much faster in $Al_2O_3/In_{0.53}Ga_{0.47}As$ compared to high-k/Si MOS devices. Source of Figure 4.13: Jacopo Franco et al [9].

4.5 Conclusions

A study of time evolution of the charge trapping in high- k /In_{0.53}Ga_{0.47}As MOS structures was performed. Based on C-V hysteresis measurements with a stress time in accumulation, it is observed in Al/Al₂O₃(8nm)/In_{0.53}Ga_{0.47}As MOS structure that the C-V hysteresis increases with a power law dependence with the stress time. In addition, charge trapping efficiency, defined as the ratio of trapped charge density to injected charge density, decreases with a power law dependence with the increasing injected charge density. Similar measurements were performed for Pd/HfO₂(15nm)/In_{0.53}Ga_{0.47}As MOS structure with a much longer stress time applied. Due to a large C-V hysteresis with $t_{\text{stress}}=0$ (i.e. ΔV_0) for HfO₂/In_{0.53}Ga_{0.47}As, $\Delta V - \Delta V_0$ is plotted and observed to increase with a power law dependence on stress time in accumulation at the initial stage of stressing and approaches to a plateau at sufficiently long stress times, consistent with trapping in pre-existing border traps which have a wide range of capture cross sections. A larger V_{max} used in the study of C-V hysteresis with a hold at V_{max} in accumulation results in a larger ΔV . This is because a larger V_{max} pushes the Fermi level further into the conduction/valence bands and also results in a larger E_{ox} which allow more border traps to be assessed.

Finally, measurements were performed to study charge trapping recovery or relaxation following stress. It is observed that a significant portion of the flatband voltage shift is recovered during the relaxation phase (1ms to 4s) after the stress voltage is removed for the HfO₂/In_{0.53}Ga_{0.47}As MOS capacitors under investigation, and as a consequence, the conventional C-V hysteresis sweeps, which can take up to one minute, underestimates the full magnitude of the trapped charge during stress. This relaxation process for the high- k /In_{0.53}Ga_{0.47}As MOS capacitors is very fast when compared to high- k /Si based MOS devices.

Bibliography

- [1] E. O'Connor, B. Brennan, V. Djara, K. Cherkaoui, S. Monaghan, S. B. Newcomb, R. Contreras, M. Milojevic, G. Hughes, M. E. Pemble, R. M. Wallace, and P. K. Hurley, *J. Appl. Phys.* **109**, 024101 (2011).
- [2] S. Zafar, A. Callegari, E. Gusev, and M. V. Fischetti, *J. Appl. Phys.* **93**, 9298 (2003).
- [3] J. Lin, Y. Y. Gomeniuk, S. Monaghan, I. M. Povey, K. Cherkaoui, E. O'Connor, M. Power, and P. K. Hurley, *J. Appl. Phys.* **114**, 144105 (2013).
- [4] J. Lin, S. Monaghan, K. Cherkaoui, I. M. Povey, E. O'Connor, B. Sheehan, and P. K. Hurley, *Microelectronic Engineering* **147**, 273–276 (2015).
- [5] S. Johansson, M. Berg, K.-M. Persson, and E. Lind, *IEEE Trans. Electron Devices*, **60**(2), 776–781 (2013).
- [6] G. Roll, J. Mo, E. Lind, S. Johansson, and L.-E. Wernersson, *Appl. Phys. Lett.* **106**, 203503 (2015).
- [7] G. Roll, J. Mo, E. Lind, S. Johansson, and L.-E. Wernersson, *IEEE Trans. Device Mater. Reliab.* **16**(2), 112–116 (2016).
- [8] A. Vais, J. Franco, H-C Lin, N. Collaert, A. Mocuta. K. De Meyer, and A. Thean, *Appl. Phys. Lett.* **107**, 233504 (2015).
- [9] J. Franco, A. Alian, B. Kaczer, D. Lin, T. Ivanov, A. Pourghaderi, K. Martens, Y. Mols, D. Zhou, N. Waldron, S. Sioncke, T. Kauerauf, N. Collaert, A. Thean, M. Heyns, G. Groeseneken, *Tech. Dig. -Int. Reliab. Phys. Symp.* 2014, 6A.2.1.

Chapter 5: Effect of Forming Gas Annealing on the Electrical Characteristics of High- k /In_{0.53}Ga_{0.47}As MOS systems

5.1 Introduction

Forming gas annealing has been reported in literature [1-4] to be effective in reducing the interface state density in high- k /In_{0.53}Ga_{0.47}As MOS systems. The primary aim of this chapter is to extend the studies of [1-4], to explore if forming gas annealing also has an effect on the border trap density which leads to C-V hysteresis. In this chapter, systematic studies of forming gas annealing (FGA) and the standard pre-ALD 10% (NH₄)₂S surface passivation (SP) on the electrical characterization of high- k /In_{0.53}Ga_{0.47}As MOS systems will be presented. Sample details will be given in section 5.2. In section 5.3, the effect of FGA at a series of temperatures on the electrical characterization of Au/Ni/high- k /In_{0.53}Ga_{0.47}As MOS structures using both HfO₂(8nm) and Al₂O₃(8nm) as the high- k oxides will be discussed. The electrical behavior including gate current density versus voltage (J-V), multi-frequency capacitance-voltage (C-V), interface state density and C-V hysteresis will all be covered. In section 5.4, a study of the effect of both FGA (one temperature) and the standard 10% (NH₄)₂S surface treatment on TiN/Al₂O₃(4nm)/In_{0.53}Ga_{0.47}As MOS structures will be discussed. Section 5.5 will conclude the whole chapter.

5.2 Sample Details

The samples studied in this chapter were heavily *n*-doped (S at $2 \times 10^{18} \text{ cm}^{-3}$) and heavily *p*-doped (Zn at $2 \times 10^{18} \text{ cm}^{-3}$) InP(100) substrates with $2 \mu\text{m}$ *n*-type (S at $4 \times 10^{17} \text{ cm}^{-3}$) and *p*-type (Zn at $4 \times 10^{17} \text{ cm}^{-3}$) $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ epitaxial layers, respectively, grown by metal organic vapour phase epitaxy (MOVPE).

The samples in this study were split into FGA temperature series (250°C to 450°C) sample set using both $\text{HfO}_2(8\text{nm})$ and $\text{Al}_2\text{O}_3(8\text{nm})$ ALD oxides and *n*- and *p*-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$. There was also a second series using $\text{Al}_2\text{O}_3(4\text{nm})$ only for *n*-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, exploring the effect of FGA at 400°C for samples with and without an initial optimised $(\text{NH}_4)_2\text{S}$ surface passivation (SP). This is referred to as the FGA/SP sample set. For the FGA temperature series sample set, the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ surfaces were all treated using the optimised 10% $(\text{NH}_4)_2\text{S}$ solution prior to ALD plus a minimum transfer time ($\sim 3\text{min}$) to the ALD chamber [5]. Either HfO_2 or Al_2O_3 were deposited on the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ by ALD. The HfO_2 dielectric has a nominal thickness of 8nm by ALD using $\text{Hf}[\text{N}(\text{CH}_3)\text{C}_2\text{H}_5]_4$ (TEMAH) and H_2O as precursors at 250°C . The Al_2O_3 dielectric also has a nominal thickness of 8nm and was deposited by ALD at 300°C using TMA and H_2O . $\text{Au}(90\text{nm})/\text{Ni}(70\text{nm})$ was used as the metal gate and was formed by electron beam evaporation and a lift-off process. After the metal deposition, the samples were treated by FGA (5% H_2 / 95% N_2) at a series of temperatures (250°C , 300°C , 350°C , 400°C and 450°C) for 30min (performed in Tyndall). One sample from each doping type and each oxide was not treated by the post-metal FGA as the control sample. The details of the FGA temperature series sample set are listed in Table 5.1. All the electrical measurements for the FGA temperature series sample set (presented in section 5.3) were carried out using E4989a LCR meter in Tyndall.

Table 5.1 FGA temperature series sample set

Substrate	Oxide	Metal	FGA condition	SP
<i>n- & p-</i> In _{0.53} Ga _{0.47} As	HfO ₂ (8nm)	Au(90nm)/Ni(70nm)	No FGA	Yes
<i>n- & p-</i> In _{0.53} Ga _{0.47} As	HfO ₂ (8nm)	Au(90nm)/Ni(70nm)	250 ⁰ C, 30min	Yes
<i>n- & p-</i> In _{0.53} Ga _{0.47} As	HfO ₂ (8nm)	Au(90nm)/Ni(70nm)	300 ⁰ C, 30min	Yes
<i>n- & p-</i> In _{0.53} Ga _{0.47} As	HfO ₂ (8nm)	Au(90nm)/Ni(70nm)	350 ⁰ C, 30min	Yes
<i>n- & p-</i> In _{0.53} Ga _{0.47} As	HfO ₂ (8nm)	Au(90nm)/Ni(70nm)	400 ⁰ C, 30min	Yes
<i>n- & p-</i> In _{0.53} Ga _{0.47} As	HfO ₂ (8nm)	Au(90nm)/Ni(70nm)	450 ⁰ C, 30min	Yes
<i>n- & p-</i> In _{0.53} Ga _{0.47} As	Al ₂ O ₃ (8nm)	Au(90nm)/Ni(70nm)	No FGA	Yes
<i>n- & p-</i> In _{0.53} Ga _{0.47} As	Al ₂ O ₃ (8nm)	Au(90nm)/Ni(70nm)	250 ⁰ C, 30min	Yes
<i>n- & p-</i> In _{0.53} Ga _{0.47} As	Al ₂ O ₃ (8nm)	Au(90nm)/Ni(70nm)	300 ⁰ C, 30min	Yes
<i>n- & p-</i> In _{0.53} Ga _{0.47} As	Al ₂ O ₃ (8nm)	Au(90nm)/Ni(70nm)	350 ⁰ C, 30min	Yes
<i>n- & p-</i> In _{0.53} Ga _{0.47} As	Al ₂ O ₃ (8nm)	Au(90nm)/Ni(70nm)	400 ⁰ C, 30min	Yes
<i>n- & p-</i> In _{0.53} Ga _{0.47} As	Al ₂ O ₃ (8nm)	Au(90nm)/Ni(70nm)	450 ⁰ C, 30min	Yes

- FGA: Post-metal forming gas annealing (5% H₂/95% N₂) (performed in Tyndall)
- SP: Pre-ALD 10% (NH₄)₂S surface passivation plus 3min transfer time to ALD chamber

For the FGA/SP sample set, only *n*-In_{0.53}Ga_{0.47}As wafers were used. Al₂O₃ of nominally 4nm was deposited by ALD at 300⁰C using TMA and H₂O. Selected In_{0.53}Ga_{0.47}As wafers were treated using the standard 10% (NH₄)₂S passivation prior to the ALD. TiN(80nm) was used as the metal gate for Al₂O₃(4nm)/*n*-In_{0.53}Ga_{0.47}As structure. TiN metal gates were deposited by sputtering and patterned using lift-off in IMEC. Selected TiN/Al₂O₃(4nm)/*n*-

In_{0.53}Ga_{0.47}As samples were treated by post-metal FGA at 400⁰C for 5min which were also performed in IMEC. The samples details are given in Table 5.2. The measurements for the FGA/SP sample set were performed in IMEC.

Table 5.2 FGA/SP sample set

Substrate	Oxide	Metal	FGA condition	SP
<i>n</i> -In _{0.53} Ga _{0.47} As	Al ₂ O ₃ (4nm)	TiN(80nm)	No FGA	No
<i>n</i> -In _{0.53} Ga _{0.47} As	Al ₂ O ₃ (4nm)	TiN(80nm)	No FGA	Yes
<i>n</i> -In _{0.53} Ga _{0.47} As	Al ₂ O ₃ (4nm)	TiN(80nm)	400 ⁰ C, 5min	No
<i>n</i> -In _{0.53} Ga _{0.47} As	Al ₂ O ₃ (4nm)	TiN(80nm)	400 ⁰ C, 5min	Yes

- FGA: Post-metal forming gas annealing (5% H₂/95% N₂) (performed in IMEC)
- SP: Pre-ALD 10% (NH₄)₂S surface passivation plus 3min transfer time to ALD chamber

5.3 Effect of FGA Temperature Series on High-*k*/In_{0.53}Ga_{0.47}As MOS Systems

5.3.1 Effect of FGA on J-V Characteristics

The gate current density versus voltage (J-V) characteristics for Au/Ni gate over HfO₂(8nm)/In_{0.53}Ga_{0.47}As and Al₂O₃(8nm)/In_{0.53}Ga_{0.47}As MOS capacitors are analyzed. A variety of sites on each sample were measured. The J-V characteristics for all samples can be found in Appendix V. All discussion is based on the “representative sites” neglecting the “outlying sites” that have very large leakage and break down at very small voltages.

a) HfO₂/In_{0.53}Ga_{0.47}As

Figure 5.1 shows J-V characteristics for Au/Ni/HfO₂(8nm)/*n*-In_{0.53}Ga_{0.47}As MOS structures treated with (a) no FGA and (b) FGA at 450⁰C, showing a dramatically increased gate current after FGA 450⁰C. Figure 5.2 illustrates the current density measured at V_g=±3V and the breakdown oxide field (E_{ox}) at both positive and negative bias. The presented data is averaged results over different measured sites. It is shown in Figure 5.2 that the gate current density increases significantly after FGA at temperatures ≥ 400⁰C and the breakdown E_{ox} is reduced after FGA at all temperatures under investigation.

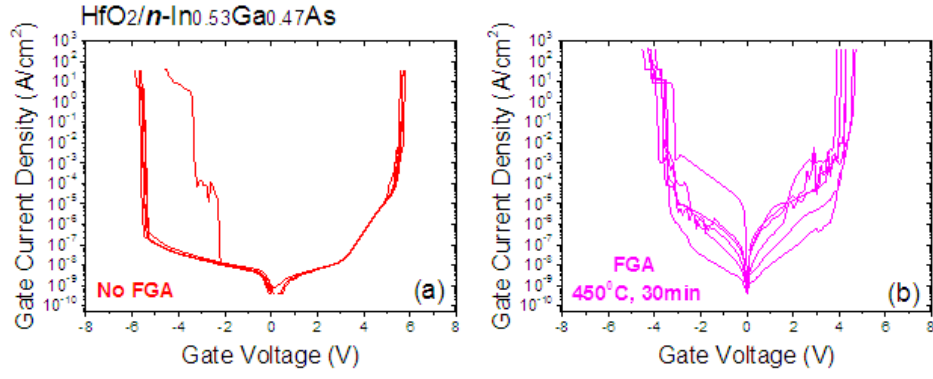


Figure 5.1: J-V characteristics at room temperature for Au/Ni/HfO₂(8nm)/n-In_{0.53}Ga_{0.47}As MOS capacitors treated with (a) no FGA and (b) FGA at 450°C. A significant increase in gate leakage is observed after FGA 450°C.

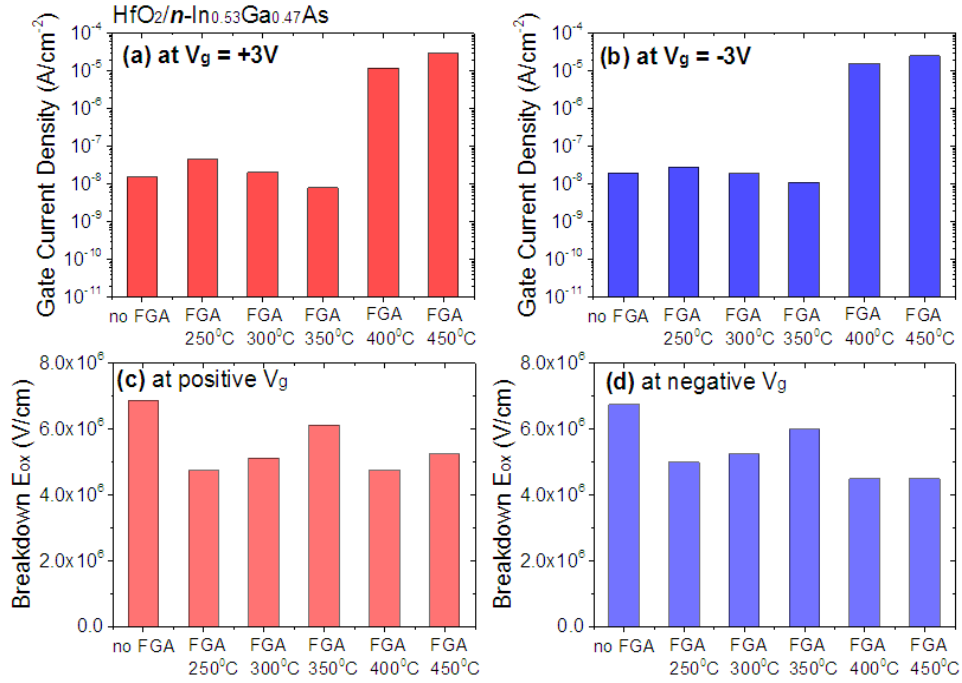


Figure 5.2: (a) Gate current density estimated at $V_g=3V$, (b) gate current density at $V_g=-3V$, (c) breakdown oxide field at positive V_g and (d) breakdown oxide field at negative V_g for Au/Ni/HfO₂(8nm)/n-In_{0.53}Ga_{0.47}As MOS capacitors. All presented data is extracted from the average of the results on a variety of sites on each sample.

J-V characteristics for the Au/Ni/HfO₂(8nm)/p-In_{0.53}Ga_{0.47}As MOS structures treated with (a) no FGA and (b) FGA at 450°C are shown in Figure 5.3, also showing that FGA 450°C results in a significant increase in gate current density. Gate current density at $V_g=\pm 3V$ and the breakdown E_{ox} are plotted in

Figure 5.4 for $\text{HfO}_2/p\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS structures. Similar to the case of $\text{HfO}_2/n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ (Figure 5.2), a significant increase in current density is observed in samples treated by $\text{FGA} \geq 400^\circ\text{C}$. The breakdown E_{ox} is found similar for different FGA conditions, in addition, no hard breakdown is observed for $\text{HfO}_2/p\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ treated with FGA 400°C and 450°C at positive bias.

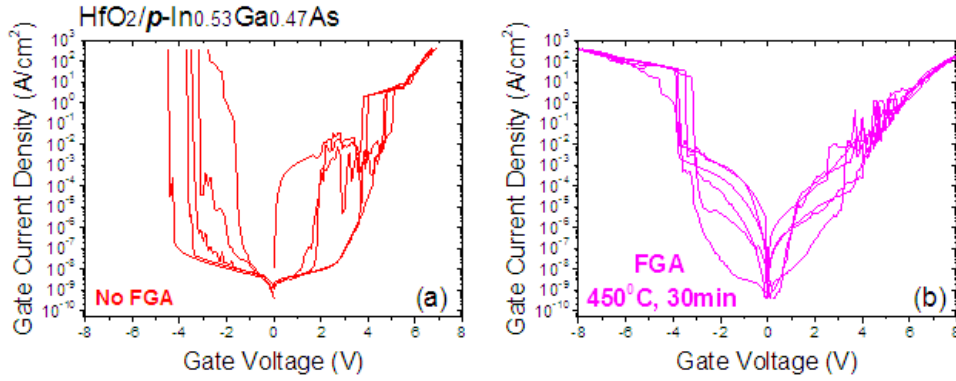


Figure 5.3: J - V characteristics at room temperature for $\text{Au/Ni/HfO}_2(8\text{nm})/p\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors treated with (a) no FGA and (b) FGA at 450°C . A significant increase in gate leakage is observed after FGA 450°C .

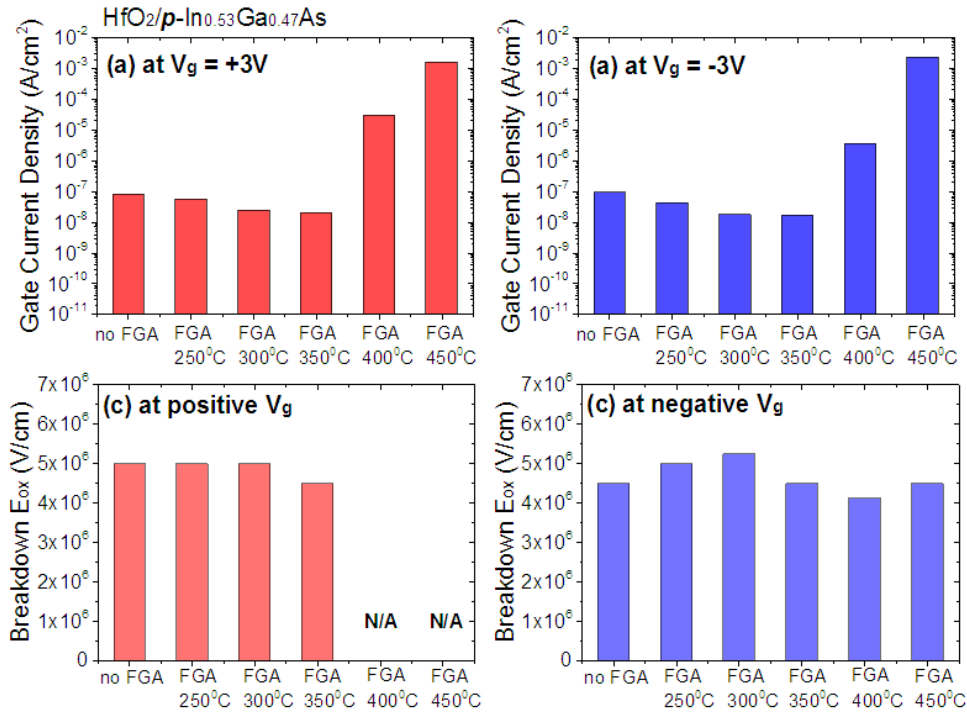


Figure 5.4: (a) Gate current density estimated at $V_g=3\text{V}$, (b) gate current density estimated at $V_g=-3\text{V}$, (c) breakdown oxide field at positive V_g and (d) breakdown oxide field at negative V_g .

breakdown oxide field at negative V_g for Au/Ni/HfO₂(8nm)/p-In_{0.53}Ga_{0.47}As MOS capacitors. All presented data is extracted from the average of the results on a variety of sites on each sample.

b) Al₂O₃/In_{0.53}Ga_{0.47}As

The J-V characteristics for Au/Ni gate Al₂O₃(8nm) over *n*-In_{0.53}Ga_{0.47}As MOS capacitors are shown in Figure 5.5. Similar to the case of HfO₂/In_{0.53}Ga_{0.47}As, gate current density is observed to increase for sample treated with FGA 450⁰C. Gate current density at $V_g = \pm 3V$ and the breakdown E_{ox} are plotted in Figure 5.6 for Al₂O₃/*n*-In_{0.53}Ga_{0.47}As MOS structures, showing that current density increases with $FGA \geq 400^0C$ and breakdown E_{ox} is found similar for different FGA conditions at both positive and negative bias.

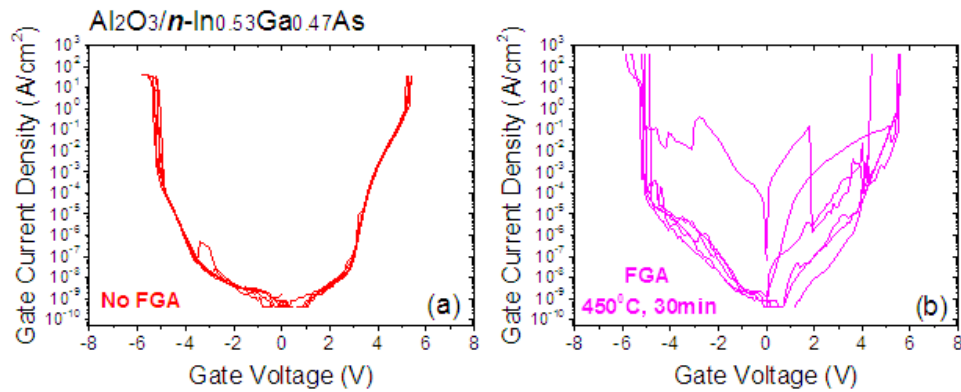


Figure 5.5: J-V characteristics at room temperature for Au/Ni/Al₂O₃(8nm)/*n*-In_{0.53}Ga_{0.47}As MOS capacitors treated with (a) no FGA and (b) FGA at 450⁰C. A significant increase in gate leakage is observed after FGA 450⁰C.

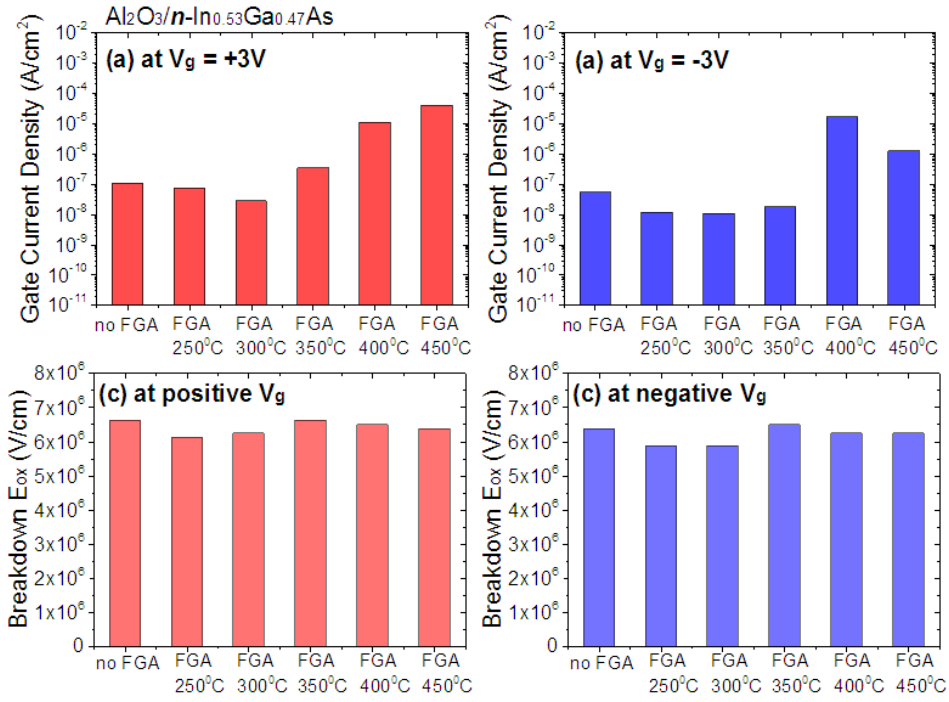


Figure 5.6: (a) Gate current density estimated at $V_g=3V$, (b) gate current density estimated at $V_g=-3V$, (c) breakdown oxide field at positive V_g and (d) breakdown oxide field at negative V_g for Au/Ni/Al₂O₃(8nm)/n-In_{0.53}Ga_{0.47}As MOS capacitors. All presented data is extracted from the average of the results on a variety of sites on each sample.

For Au/Ni/Al₂O₃(8nm)/p-In_{0.53}Ga_{0.47}As MOS structures (Figure 5.7 and Figure 5.8), the J-V characteristics for FGA at all temperatures have very similar behaviors (current density and breakdown E_{ox}) except for FGA 400⁰C which exhibits increased leakage compared to other samples. It has been noted in the measurements that FGA 400⁰C on Al₂O₃ samples (both *n*- and *p*-type In_{0.53}Ga_{0.47}As) have shown non-regular behavior. This is will be discussed in the next section.

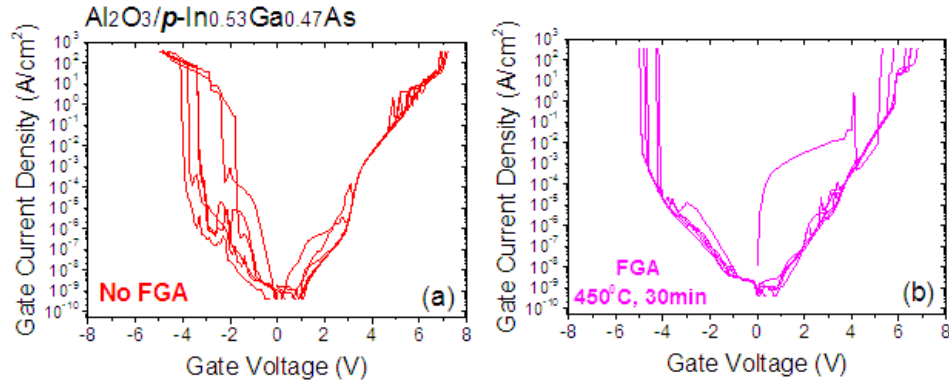


Figure 5.7: J-V characteristics at room temperature for Au/Ni/Al₂O₃(8nm)/p-In_{0.53}Ga_{0.47}As MOS capacitors treated with (a) no FGA and (b) FGA at 450°C.

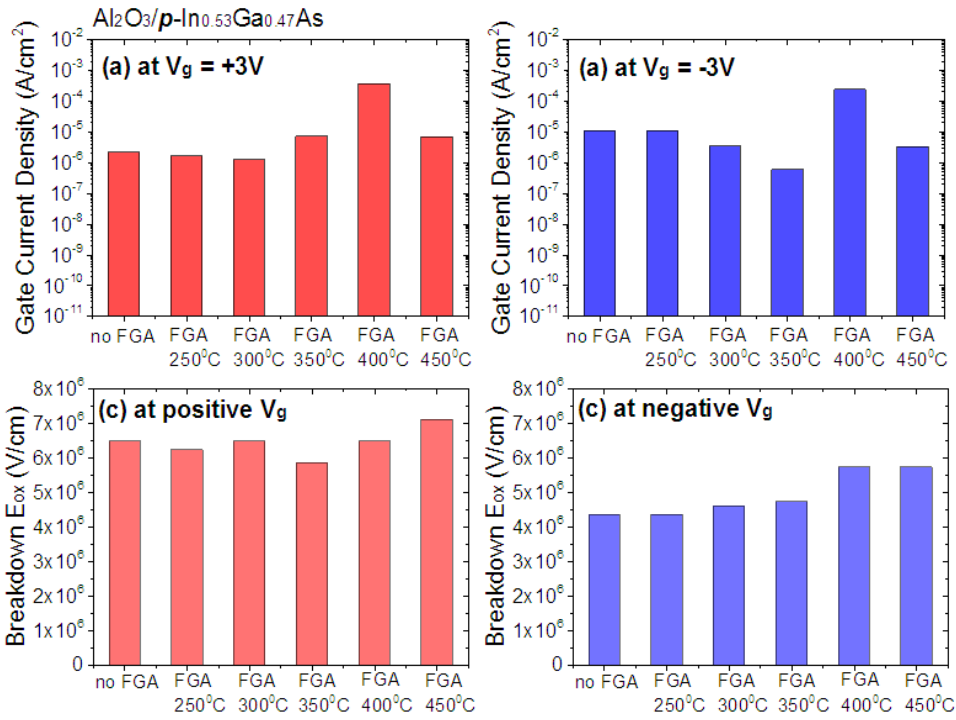


Figure 5.8: (a) Gate current density estimated at $V_g=3V$, (b) gate current density estimated at $V_g=-3V$, (c) breakdown oxide field at positive V_g and (d) breakdown oxide field at negative V_g for Au/Ni/Al₂O₃(8nm)/p-In_{0.53}Ga_{0.47}As MOS capacitors. All presented data is extracted from the average of the results on a variety of sites on each sample.

To conclude, for HfO₂/n-In_{0.53}Ga_{0.47}As, HfO₂/p-In_{0.53}Ga_{0.47}As and Al₂O₃/n-In_{0.53}Ga_{0.47}As MOS structures, an increase in leakage current following FGA $\geq 400^\circ\text{C}$ are observed. For the Al₂O₃/p-In_{0.53}Ga_{0.47}As, an increase in leakage

is only observed in FGA 400⁰C sample but not the FGA 450⁰C sample. The C-V characteristics, which will be discussed in the following sections, were measured within the bias range avoiding getting close to the breakdown voltages observed in the J-V measurements.

5.3.2 Effect of FGA on C-V characteristics and D_{it}

a) $HfO_2/In_{0.53}Ga_{0.47}As$

The multi-frequency (20Hz~1MHz) C-V characteristics measured at room temperature for $Au/Ni/HfO_2(8nm)/n-In_{0.53}Ga_{0.47}As$ MOS structure treated with different FGA conditions are illustrated in Figure 5.9. Firstly, it is observed that the maximum capacitance (C_{max}) measured at the maximum voltage (V_{max}) in accumulation is increased after FGA at all the temperatures under study compared to the sample with no FGA. Secondly, the C-V responses exhibit a sharper transition from inversion to accumulation after FGA at all the temperatures under investigation, indicating that FGA at these temperatures is effective in reducing the interface states which result in less stretch-out in the C-V characteristics.

Moreover, the capacitance measured in the bias range $V_g = -2.5V$ to $-1V$ for the no FGA sample and FGA 250⁰C sample is not representative of true inversion. True inversion at the high- $k/In_{0.53}Ga_{0.47}As$ interface would result in a constant capacitance as a function of gate voltage for all measurement frequencies; however, it is observed in the C-V responses for no FGA and FGA 250⁰C samples that the capacitance keeps increasing with the negatively increasing gate voltage, which can be a result of C-V stretch-out from a wide interface state distribution. For the samples treated with FGA 300⁰C to 450⁰C, the capacitance measured at intermediate frequencies clearly go through a peak and then decrease and is very likely reaching a constant value if the gate voltage keeps increasing negatively. Finally, the frequency dispersion estimated at V_{max} is investigated. Frequency dispersion is based on the dispersion (% per decade) between high frequency of 1MHz and low frequency of 40Hz instead of 20Hz as the measured capacitance at 20Hz is noisy. The frequency dispersion (at V_{max}) is a result of the combination of

interface states near and/or inside the bands and border traps with energy levels near the band edges [6-8]. It is observed that the frequency dispersion is improved after FGA at all temperatures and the frequency dispersion is the smallest for FGA at 350°C and increases towards both lower and higher FGA temperatures for $\text{HfO}_2/n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS structure (see Figure 5.10).

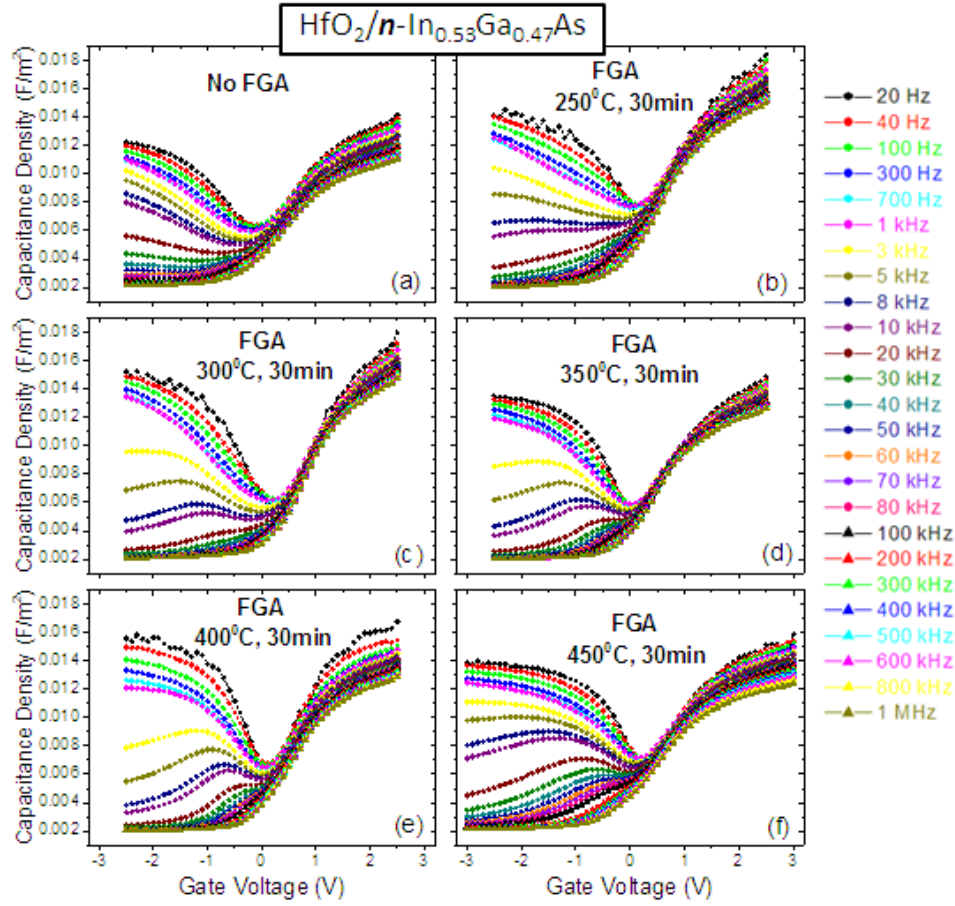


Figure 5.9: Multi-frequency (20Hz-1MHz) C-V characteristics at room temperature for $\text{Au/Ni/HfO}_2(8\text{nm})/n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors treated by different FGA conditions.

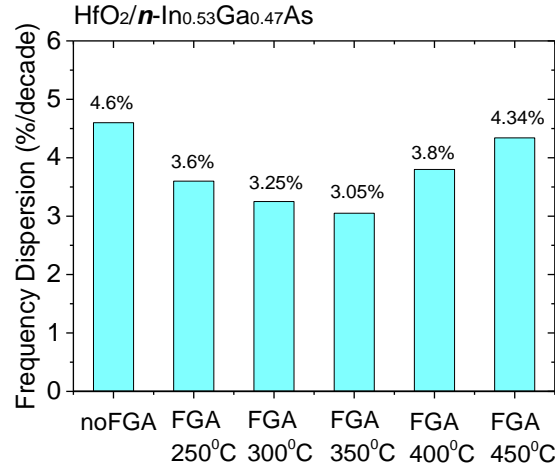


Figure 5.10: Frequency dispersion estimated at V_{max} in accumulation as a function of FGA condition for $Au/Ni/HfO_2(8nm)/n-In_{0.53}Ga_{0.47}As$ MOS capacitors.

For $Au/Ni/HfO_2(8nm)/p-In_{0.53}Ga_{0.47}As$ MOS structure illustrated in Figure 5.11, the multi-frequency C-V characteristics are all degraded when compared to the case of $HfO_2/n-In_{0.53}Ga_{0.47}As$ (see Figure 5.9), this is the most noticeable in the nominal accumulation region at negative gate voltage for $p-In_{0.53}Ga_{0.47}As$. This is consistent with an increase in interface state density (D_{it}) towards the valance band edge as previously published [9, 10]. As shown in Figure 5.12, an improvement in frequency dispersion at V_{max} is observed at FGA 250°C, 300°C and 350°C. FGA at high temperatures (i.e. 400°C and 450°C) increase the frequency dispersion. For no FGA, FGA 400°C and 450°C samples at their corresponding V_{max} and 1MHz, the flatband capacitance is not reached, suggesting that the Fermi level movement in the $In_{0.53}Ga_{0.47}As$ lower bandgap is strongly restricted and thus the Fermi level cannot move into the valence band edge to accumulate holes. The accumulation-like capacitance measured at low frequencies is a consequence of a capacitance contribution of an interface state capacitance (C_{it}) in parallel with the differential capacitance (C_s) of the $In_{0.53}Ga_{0.47}As$. As C_{it} is large compared to C_s and C_{ox} , according to the equivalent circuit of a MOS capacitor with the presence of interface states which were discussed in chapter 2 (see Figure 2.11 and equation (2.11)), measured capacitance at low frequency can approach C_{ox} but this does not indicate that accumulation is

achieved. This behavior is very similar to the multi-frequency C-V characteristics for high- k oxide on n -type GaAs MOS system where the Fermi level is almost pinned in the upper bandgap of GaAs resulting in a significant level of frequency dispersion at V_{\max} [11].

Considering the C-V responses in the nominal inversion region, good inversion behavior is observed for all the samples except for the FGA 450⁰C sample as the capacitance for the no FGA and FGA (250⁰C to 400⁰C) samples is almost reaching a plateau with the positively increasing gate voltage, which indicates a low interface state density distributed in the In_{0.53}Ga_{0.47}As upper band for these samples. The decrease in capacitance at low frequencies at $V_g \approx 1\text{V}$ to 2V observed in Figure 5.11(f) for FGA 450⁰C sample is most probably due to the large increase in the average leakage current density at +2V for this sample following the 450⁰C FGA anneal (see Figure 5.3 (b)). Due to the high leakage current density for the 450⁰C anneal samples at +2V (up to $\sim 10^{-4}\text{A/cm}^2$), the inversion layer cannot be sustained, leading to a decrease in capacitance.

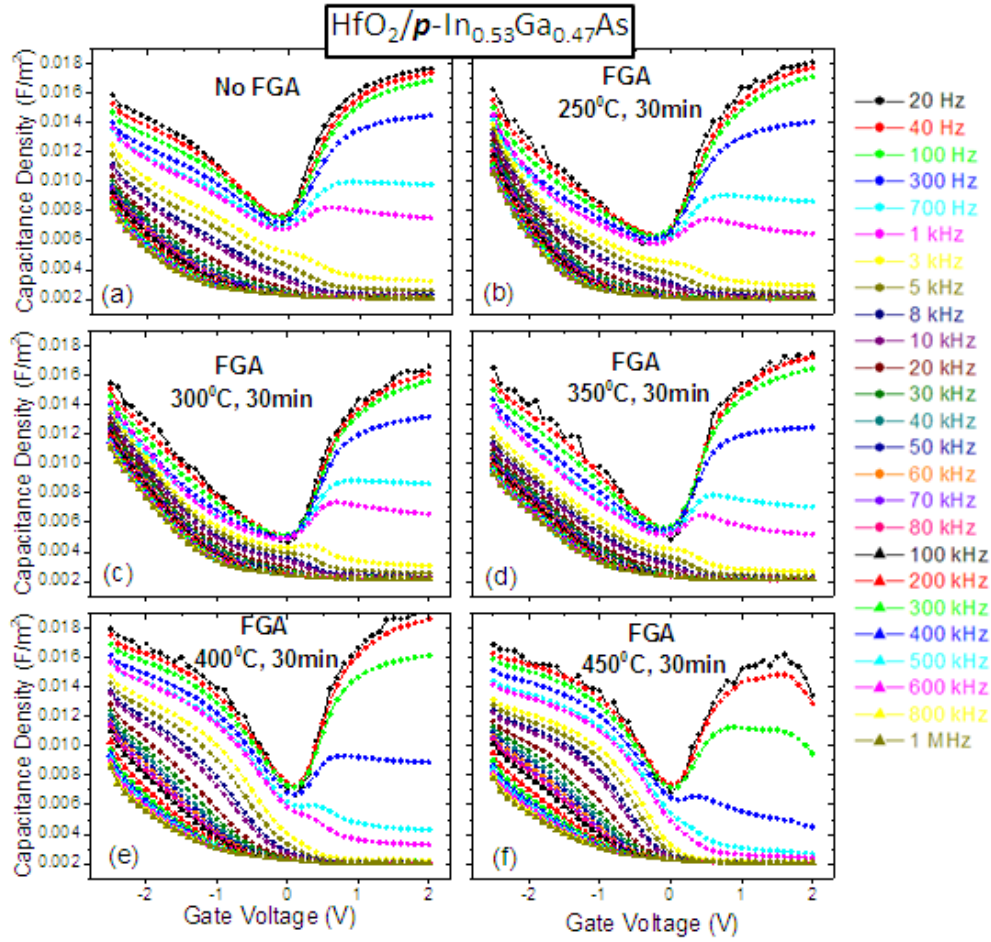


Figure 5.11: Multi-frequency (20Hz-1MHz) C-V characteristics at room temperature for Au/Ni/HfO₂(8nm)/p-In_{0.53}Ga_{0.47}As MOS capacitors treated by different FGA conditions.

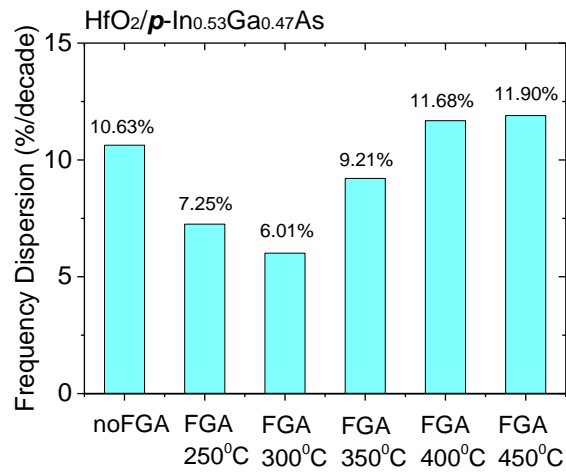


Figure 5.12: Frequency dispersion estimated at V_{max} in accumulation as a function of FGA condition for Au/Ni/HfO₂(8nm)/p-In_{0.53}Ga_{0.47}As MOS capacitors.

Interface state density (D_{it}) is estimated using high-low frequency capacitance method. Due to the relatively high noise level observed at the lowest frequency (i.e. 20Hz), C-V measured at 40Hz is used as the low frequency C-V for the D_{it} extraction. The D_{it} is extracted at a gate voltage in depletion where minority carrier responses with interface states are the minimum, and majority carrier interaction with border traps located at energies aligned with the conduction or valence bands can be neglected. In order to estimate the corresponding interface state energy level in the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ bandgap, C-V measured at the highest frequency and lowest temperature possible or a simulation of the theoretical high frequency is needed as the measured 1MHz C-V at room temperature (RT) cannot be representative of a perfect true high frequency C-V characteristic. If the measured 1MHz RT C-V is used, this may result in a large error in the calculation of D_{it} energy levels especially for the case of high D_{it} MOS systems such as $\text{HfO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, in which case interface state responses are not completely suppressed (i.e. $C_{it} \neq 0$). The calculation of D_{it} energy levels is beyond the scope of this study and will be included in the future work (see Chapter 7).

Table 5.3 listed the D_{it} for the Au/Ni gate HfO_2 over n -type and p -type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS systems. The D_{it} values shown in Table 5.3 were extracted at V_g values where both the effect of majority and minority carriers are minimum. For $\text{HfO}_2/n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$, samples treated by FGA at 300⁰C and 350⁰C have lower D_{it} than the other FGA conditions, which is consistent with the much improved C-V responses in depletion region for these two FGA temperatures illustrated in Figure 5.9. For $\text{HfO}_2/p\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$, FGA at 300⁰C has the lowest D_{it} value which is consistent with the multi-frequency C-V shown in Figure 5.11, where the C-V characteristic is much less stretched-out than the other FGA conditions.

Table 5.3 Interface state density ($\text{cm}^{-2}\text{eV}^{-1}$) for Au/Ni/HfO₂(8nm)/In_{0.53}Ga_{0.47}As MOS systems using high-low frequency capacitance method. D_{it} values were estimated at gate voltages where the effect of majority and minority carriers are minimum.

Sample	No FGA	FGA 250 ⁰ C	FGA 300 ⁰ C	FGA 350 ⁰ C	FGA 400 ⁰ C	FGA 450 ⁰ C
HfO ₂ / <i>n</i>	2.70x10 ¹² (V _g =0.2V)	3.00x10 ¹² (V _g =0.5V)	1.62x10 ¹² (V _g =0.6V)	1.25x10 ¹² (V _g =0.4V)	3.00x10 ¹² (V _g =0.3V)	2.04x10 ¹² (V _g =0.5V)
HfO ₂ / <i>p</i>	6.61x10 ¹² (V _g =-0.1V)	4.49x10 ¹² (V _g =-0.2V)	2.65x10 ¹² (V _g =0V)	3.38x10 ¹² (V _g =-0.1V)	6.03x10 ¹² (V _g =-0.1V)	6.13x10 ¹² (V _g =0V)

b) Al₂O₃/In_{0.53}Ga_{0.47}As

The multi-frequency (20Hz~1MHz) C-V characteristics measured at room temperature for Au/Ni/Al₂O₃(8nm)/*n*-In_{0.53}Ga_{0.47}As are illustrated in Figure 5.13. It is observed in Figure 5.13 that FGA at all temperatures improve the C-V responses in terms of the transition from inversion to accumulation compared to the no FGA sample. As shown in Figure 5.14, the frequency dispersion at V_{max} is improved following all the FGA temperatures except for FGA 400⁰C which is 3.17%/decade compared to 2.92%/decade for the no FGA sample. As the FGA 400⁰C sample does not show regular behavior, possibly because FGA process went wrong (e.g. lack of forming gas or non-uniformity in temperature) on this sample, this sample has been omitted from the FGA temperature series in terms of determining general trends for the evolution of the impedance response with FGA temperature. In this case, in Figure 5.14, accumulation frequency dispersion decreases with increasing FGA temperature for Al₂O₃/*n*-In_{0.53}Ga_{0.47}As MOS structure.

For the no FGA sample presented in Figure 5.13(a), there are no observable C_{it} “bumps” near the transition region between depletion and inversion, and the capacitance measured at all frequencies tend to reach a plateau further into inversion. Interface states can have a broad distribution in the bandgap which can result in very broad C_{it} “bumps” and C-V stretch-out, making it more likely that the C_{it} “bumps” are lost in the C-V where minority carrier responses start to take over, especially in the case of Al₂O₃/In_{0.53}Ga_{0.47}As

MOS system with relatively low D_{it} level. Even though a constant capacitance as a function of negatively increasing V_g in the nominal inversion region is observed, this is not a perfect representation of true inversion being reached. In order to verify that true inversion is reached, one approach is to do capacitance (C) versus frequency (ω) and conductance (G_m) versus frequency measurements and compare the $-\omega \cdot dC/d\omega$ versus ω and G_m/ω versus ω plots at strong inversion voltages to the simulated/theoretical curves [12]. This is out of the scope of this thesis.

Following FGA at 250⁰C, 300⁰C and 350⁰C, the C-V is less stretched-out and C_{it} “bumps” become visible compared to the no FGA sample. For FGA temperature from 250⁰C increased to 350⁰C, there is a reduced response of interface states in terms of the magnitude and width of the C_{it} “bumps” with the increasing FGA temperature. For the sample treated by FGA 400⁰C, in addition to the unexpected increased accumulation frequency dispersion discussed earlier, the inversion behavior is also degraded; this is again indicating that FGA 400⁰C process may have gone wrong. The sample treated by FGA 450⁰C exhibits the best C-V characteristic which shows very small stretch-out in the C-V, the lowest level of accumulation frequency dispersion and the excellent inversion behavior. The “bumps” observed in the FGA 450⁰C sample is unlikely to be caused by interface states, instead it is a transition behavior which is also observed in theoretical C-V responses simulated with no D_{it} at all [12].

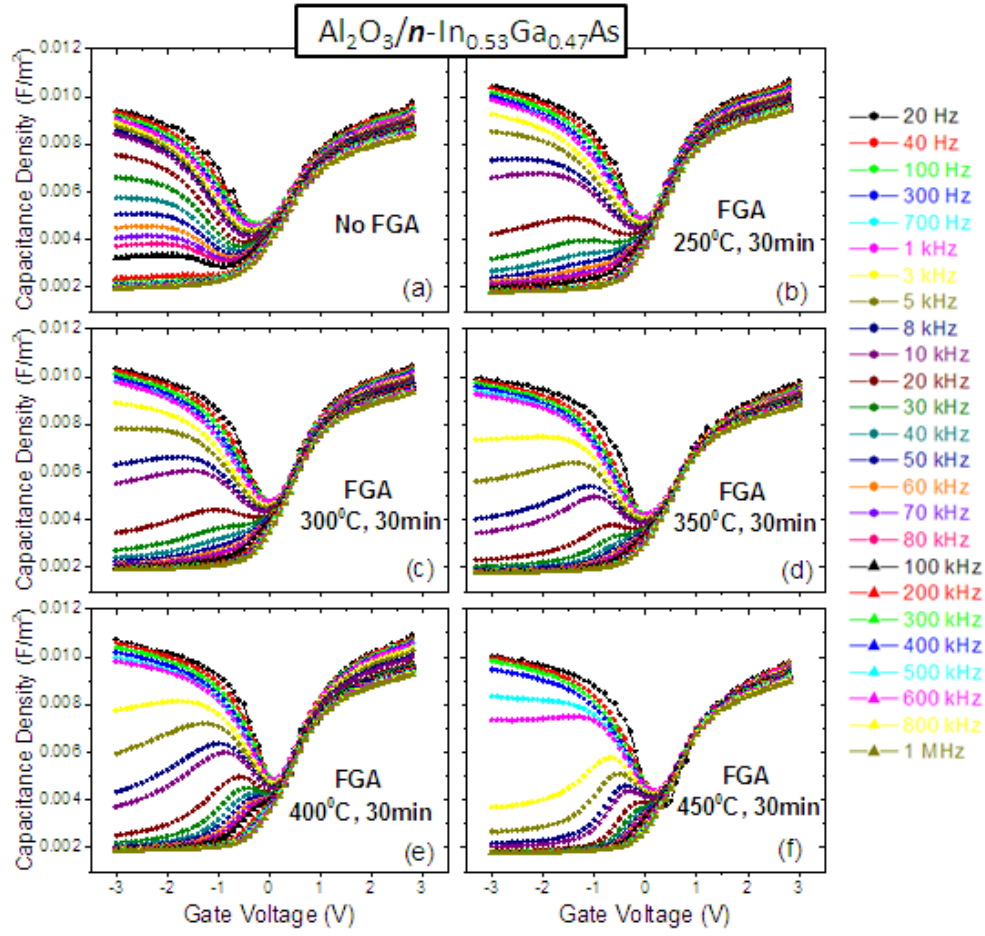


Figure 5.13: Multi-frequency (20Hz-1MHz) C-V characteristics at room temperature for Au/Ni/Al₂O₃(8nm)/n-In_{0.53}Ga_{0.47}As MOS capacitors treated by different FGA conditions.

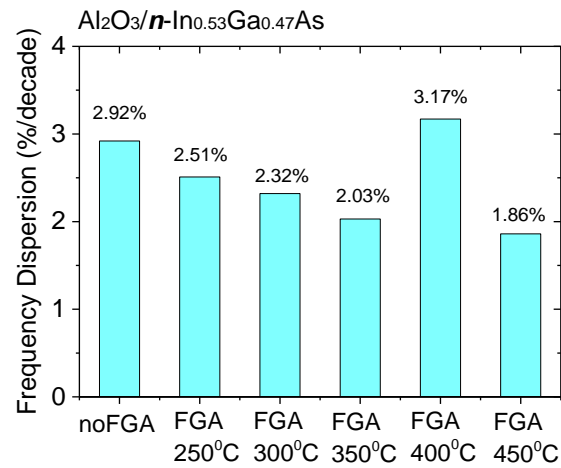


Figure 5.14: Frequency dispersion estimated at V_{max} in accumulation as a function of FGA condition for Au/Ni/Al₂O₃(8nm)/n-In_{0.53}Ga_{0.47}As MOS capacitors. Note that the FGA 400°C sample is an outlier.

The multi-frequency (20Hz~1MHz) C-V characteristics measured at room temperature for Au/Ni/Al₂O₃(8nm)/p-In_{0.53}Ga_{0.47}As are illustrated in Figure 5.15. The corresponding frequency dispersion (at V_{max}) in accumulation is shown in Figure 5.16. For Al₂O₃/p-In_{0.53}Ga_{0.47}As MOS systems, the frequency dispersion at V_{max} is larger than the case of Al₂O₃/n-In_{0.53}Ga_{0.47}As, as expected due to the high D_{it} in the lower bandgap than that in the upper bandgap in high-*k*/In_{0.53}Ga_{0.47}As MOS systems. It is also observed that there is no significant improvement in the accumulation frequency dispersion nor the C-V stretch-out following the FGA for Al₂O₃/p-In_{0.53}Ga_{0.47}As MOS structure. Similar to the case of Al₂O₃/n-In_{0.53}Ga_{0.47}As, FGA at 400°C increases the accumulation frequency dispersion and degraded the inversion behavior for Al₂O₃/p-In_{0.53}Ga_{0.47}As MOS structure.

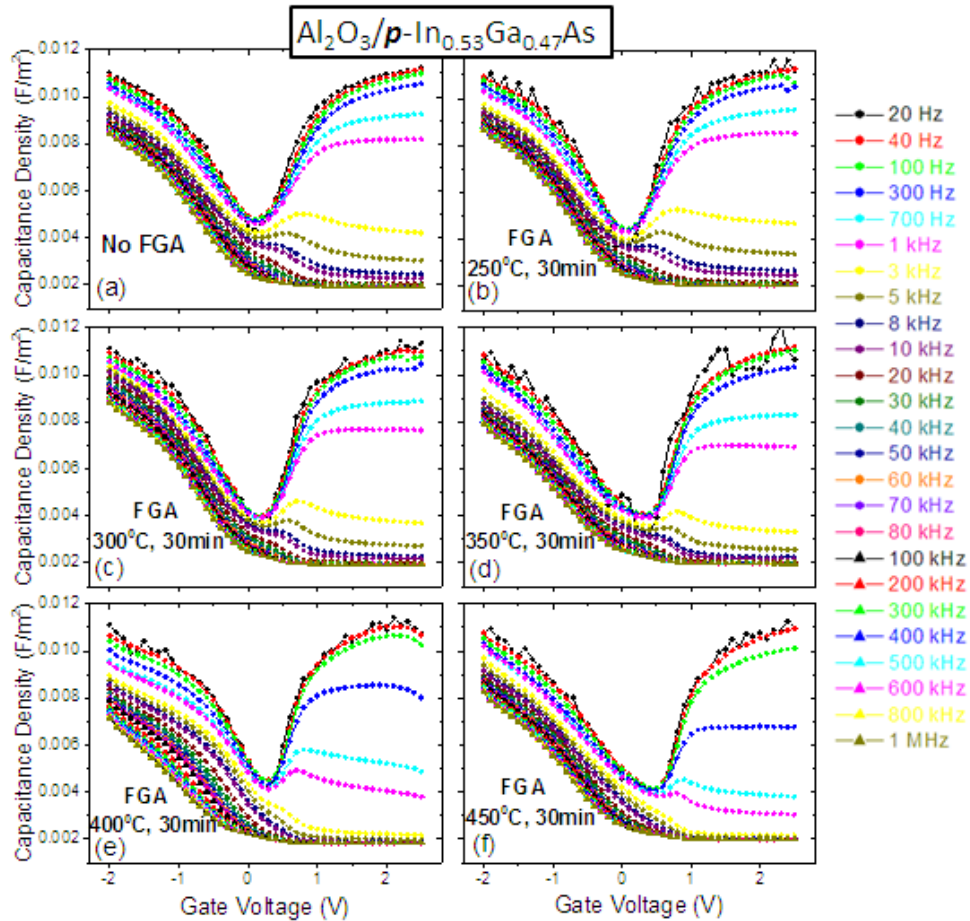


Figure 5.15: Multi-frequency (20Hz-1MHz) C-V characteristics at room temperature for Au/Ni/Al₂O₃(8nm)/p-In_{0.53}Ga_{0.47}As MOS capacitors treated by different FGA conditions.

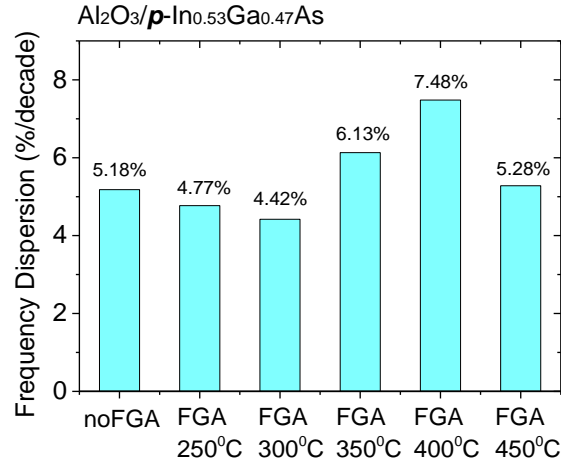


Figure 5.16: Frequency dispersion estimated at V_{max} in accumulation as a function of FGA condition for $Au/Ni/Al_2O_3(8nm)/p-In_{0.53}Ga_{0.47}As$ MOS capacitors. Note that the FGA 400°C sample is an outlier.

The high-low frequency capacitance method is also applied to $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOS systems and D_{it} for the samples under each FGA condition is summarized in Table 5.4. FGA at 450°C on Al_2O_3 n -type sample results in a very low value of D_{it} of only $2.19 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$, which is one order of magnitude lower than the n -type sample with no FGA and this is consistent with the best multi-frequency C-V characteristics shown in Figure 5.13(f) compared to other FGA conditions. For Al_2O_3 p -type sample, according to D_{it} values, there is no significant improvement after FGA at all temperatures.

Table 5.4 Interface state density ($\text{cm}^{-2} \text{ eV}^{-1}$) for $Au/Ni/Al_2O_3(8nm)/In_{0.53}Ga_{0.47}As$ MOS systems using high-low frequency capacitance method. D_{it} values were estimated at gate voltages where the effect of majority and minority carriers are minimum.

Sample	No FGA	FGA 250°C	FGA 300°C	FGA 350°C	FGA 400°C	FGA 450°C
Al_2O_3 / n	2.20×10^{12} ($V_g=0.1V$)	2.21×10^{12} ($V_g=0.1V$)	1.73×10^{12} ($V_g=0.2V$)	9.47×10^{11} ($V_g=0.5V$)	1.43×10^{12} ($V_g=0.3V$)	2.19×10^{11} ($V_g=0.7V$)
Al_2O_3 / p	4.12×10^{12} ($V_g=0.1V$)	3.06×10^{12} ($V_g=0V$)	2.38×10^{12} ($V_g=0.1V$)	2.56×10^{12} ($V_g=0.3V$)	3.71×10^{12} ($V_g=0.3V$)	2.83×10^{12} ($V_g=0.4V$)

5.3.3 Effect of FGA on C-V Hysteresis

In this section, the effect of FGA temperature on C-V hysteresis (or charge trapping) for Au/Ni gate over $\text{HfO}_2(8\text{nm})/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and $\text{Al}_2\text{O}_3(8\text{nm})/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS systems will be analyzed. All the C-V hysteresis measurements were performed at 1MHz and room temperature in order to minimize the C_{it} contribution to the overall measured capacitance of the MOS capacitors. Charge trapping density is calculated using $Q_{\text{trapped}} = C_{\text{ox}}\Delta V/q$, where ΔV is flatband voltage (V_{fb}) shift estimated at the nominal flatband capacitance. For each MOS structure, C-V hysteresis was measured with the same starting DC bias point in inversion and an increasing maximum DC bias point in accumulation (V_{max}). For each bias range, a fresh device was used. C-V hysteresis is investigated as a function of overdrive voltage (V_{ov}), where $V_{\text{ov}} = |V_{\text{max}} - V_{\text{fb}}|$. For all the samples under investigation, the $n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ samples exhibit positive voltage shift in the C-V hysteresis and the $p\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ samples exhibit negative voltage shift in the C-V hysteresis, thus indicating electrons trapping and holes trapping occurring the n -type and p -type sample, respectively.

a) $\text{HfO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$

C-V hysteresis (ΔV) and the corresponding charge trapping density (Q_{trapped}) as a function of overdrive voltage (V_{ov}) for Au/Ni/ $\text{HfO}_2(8\text{nm})/n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors with different FGA conditions are shown in Figure 5.17 (a) and (b), respectively. Compared to the no FGA sample (shown in red), the C-V hysteresis is reduced after FGA at all temperatures within the V_{ov} values investigated except for FGA 400°C (shown in magenta), which is almost overlapping the red curve for the no FGA sample.

As observed in Figure 5.17, the slope of the plot of ΔV (or Q_{trapped}) as a function of V_{ov} is different between samples with different FGA conditions. In this study, voltage acceleration factor, denoted as γ , is defined as the slope of C-V hysteresis (or Q_{trapped}) versus V_{ov} . Voltage acceleration factor as a function of FGA conditions is plotted in Figure 5.18 for the $\text{HfO}_2/n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS structure. γ -factor is an indication of the energy spread of

the border traps energy levels near/at the oxide/semiconductor interface. Different γ -factors will affect C-V hysteresis extracted at different V_{ov} values, which will make the comparison of ΔV between samples very complicated. For example, the FGA 450⁰C sample exhibits the smallest γ , and this will result in relatively low value of ΔV at a higher V_{ov} (or at higher oxide field (E_{ox})) compared to the other samples. However, at very low V_{ov} values (i.e. under low E_{ox}), ΔV for the FGA 450⁰C sample can be larger than other samples which have larger γ -factors. Figure 5.19 illustrates C-V hysteresis as a function of FGA conditions for HfO₂/n-In_{0.53}Ga_{0.47}As MOS structure at $V_{ov} = 1V, 2V$ and $3V$.

Increased γ -factor is expected for improved device reliability [13, 14]. For instance, in the case of HfO₂/n-In_{0.53}Ga_{0.47}As MOS structure, the sample treated by the highest FGA temperature (i.e. 450⁰C) exhibits the smallest γ -factor compared to other FGA conditions, indicating that FGA at 450⁰C results in a wider distribution of the oxide trap defect levels. This leads to an increased ΔV at low V_{ov} or E_{ox} (e.g. $V_{ov}=1V$, see Figure 5.19), which is a degraded reliability projection at low operating voltage. The HfO₂/n-In_{0.53}Ga_{0.47}As samples treated with intermediate temperatures (i.e. 300⁰C and 350⁰C) exhibit improved γ -factor, indicating that FGA at 300⁰C and 350⁰C passivate the tails of a normal distribution of defects as illustrated in Figure 5.20, this will reduce the trapped charge in the range of Fermi level movement (at low E_{ox}).

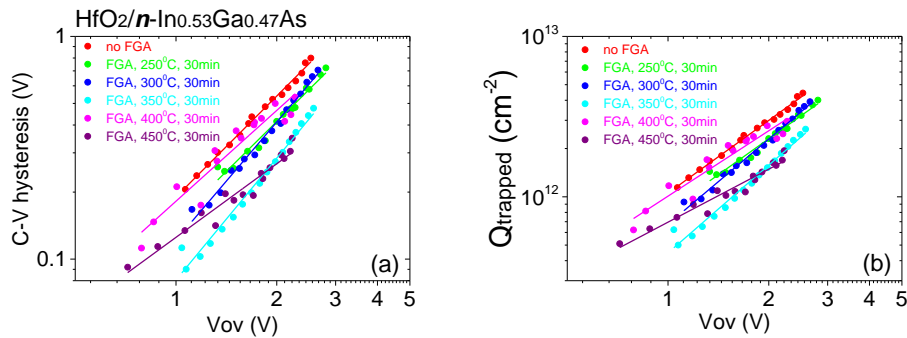


Figure 5.17: (a) C-V hysteresis and (b) the corresponding charge trapping density as a function of overdrive voltage for Au/Ni/HfO₂(8nm)/n-In_{0.53}Ga_{0.47}As MOS capacitors.

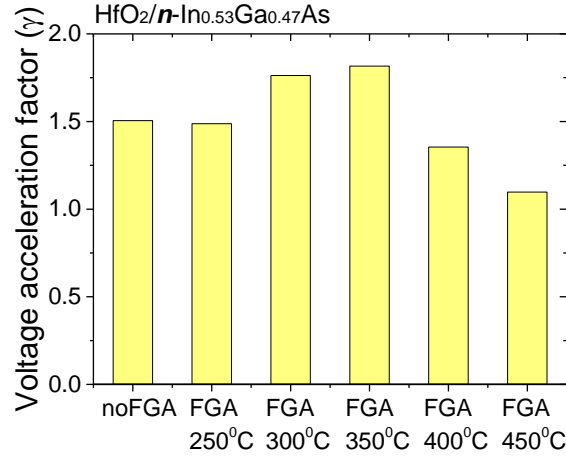


Figure 5.18: Voltage acceleration factor for Au/Ni/HfO₂(8nm)/n-In_{0.53}Ga_{0.47}As MOS capacitors.

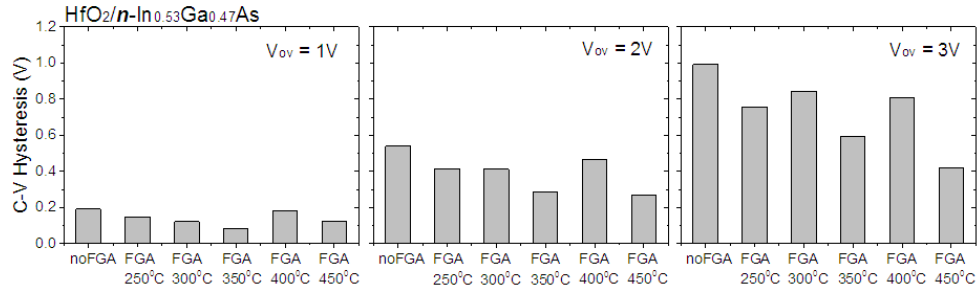


Figure 5.19: C-V hysteresis for Au/Ni/HfO₂(8nm)/n-In_{0.53}Ga_{0.47}As MOS capacitors at V_{ov} = 1V, 2V and 3V.

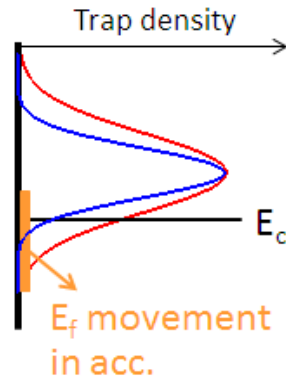


Figure 5.20: Wide (red) and narrow (blue) normal distribution of border trap density. It is noted that reduced spread of the defect distribution (blue) results in reduced trap density accessed at low E_{ox} , which is an indication of reduced device instability.

For the case of Au/Ni/HfO₂(8nm)/p-In_{0.53}Ga_{0.47}As MOS structure shown in Figure 5.21, for the no FGA sample and the FGA 450⁰C sample, flatband condition can be hardly reached therefore the presented C-V hysteresis is estimated at half the maximum capacitance ($C_{\max}/2$) and exhibit relatively small charge trapping as the holes cannot be accumulated at the In_{0.53}Ga_{0.47}As surface. Due to the poor electrical behaviour of HfO₂/p-In_{0.53}Ga_{0.47}As MOS systems, it is difficult to draw conclusion whether or not the FGA has any effect on charge trapping as the no FGA and FGA 450⁰C cannot reach flatband condition making it difficult to compare all C-V hysteresis under the same oxide field. For those HfO₂/p-In_{0.53}Ga_{0.47}As samples where flatband capacitance can be reached (FGA 250⁰C~400⁰C) in the 1MHz C-V hysteresis measurement, FGA 300⁰C sample exhibits the most improved γ -factor thus reducing ΔV at low V_{ov} (see Figure 5.22 and Figure 5.23 omitting the no FGA and FGA 450⁰C samples).

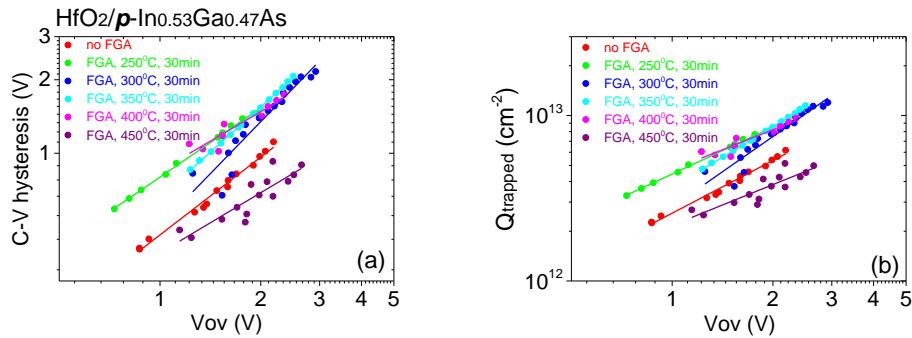


Figure 5.21: (a) C-V hysteresis and (b) the corresponding charge trapping density as a function of overdrive voltage for Au/Ni/HfO₂(8nm)/p-In_{0.53}Ga_{0.47}As MOS capacitors.

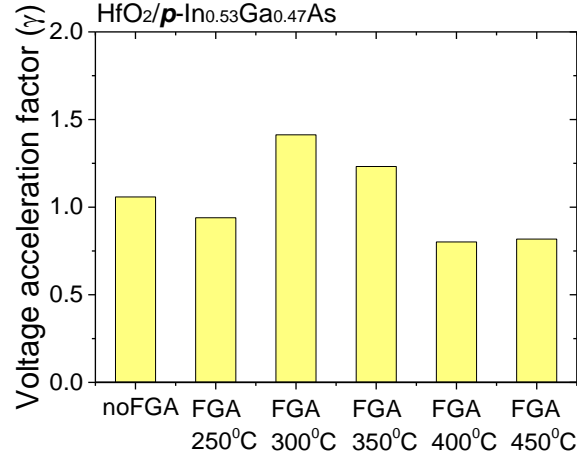


Figure 5.22: Voltage acceleration factor for Au/Ni/HfO₂(8nm)/p-In_{0.53}Ga_{0.47}As MOS capacitors.

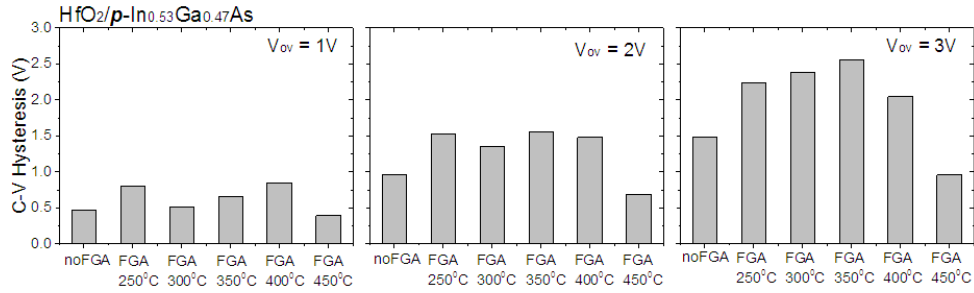


Figure 5.23: C-V hysteresis for Au/Ni/HfO₂(8nm)/p-In_{0.53}Ga_{0.47}As MOS capacitors at $V_{ov} = 1V$, $2V$ and $3V$.

b) Al₂O₃/In_{0.53}Ga_{0.47}As

Similar to previous sections in the discussion of Al₂O₃/In_{0.53}Ga_{0.47}As, FGA 400°C is omitted. C-V hysteresis and the corresponding charge trapping density as a function of overdrive voltage for Au/Ni gate Al₂O₃(8nm)/n-In_{0.53}Ga_{0.47}As MOS capacitors are shown in Figure 5.24, and the extracted γ -factors are shown in Figure 5.25. There is a slight variation of γ -factor throughout all FGA conditions. FGA 350°C sample exhibits slightly improved γ -factor compared to other samples. Figure 5.26 illustrates ΔV extracted at $V_{ov} = 1V$, $2V$ and $3V$, showing that ΔV is reduced after FGA at all temperatures at all three V_{ov} values. Assuming γ -factors are all the same, FGA at all the temperatures under investigation reduce the C-V hysteresis and there is no significant difference in C-V hysteresis between different

FGA temperatures for $\text{Al}_2\text{O}_3/\text{n-In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS structure. These observations suggest that the annealing is reducing the total density of border traps while the distribution of defect energy levels remains the same.

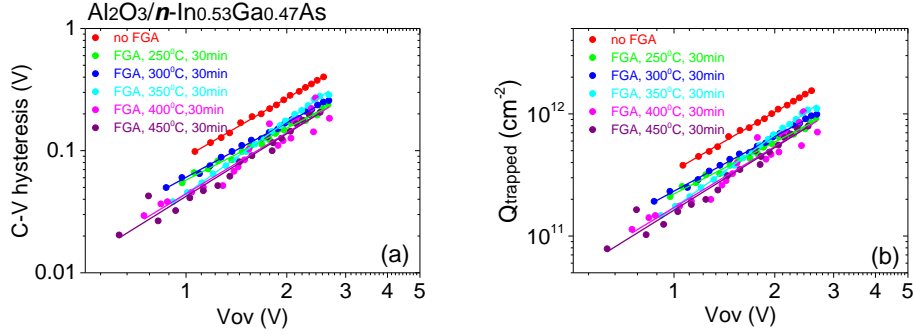


Figure 5.24: (a) C-V hysteresis and (b) the corresponding charge trapping density as a function of overdrive voltage for $\text{Au/Ni/Al}_2\text{O}_3(8\text{nm})/\text{n-In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors.

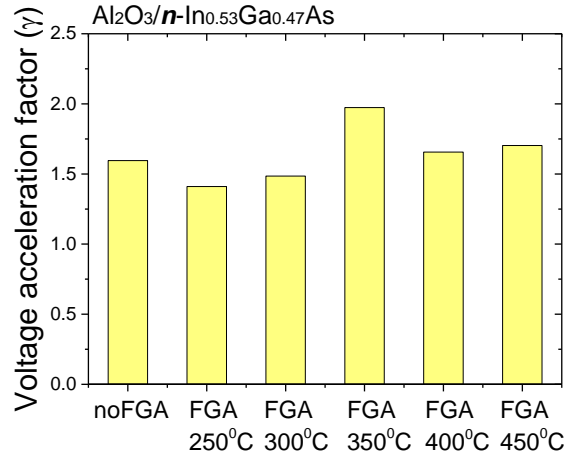


Figure 5.25: Voltage acceleration factor for $\text{Au/Ni/Al}_2\text{O}_3(8\text{nm})/\text{n-In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors.

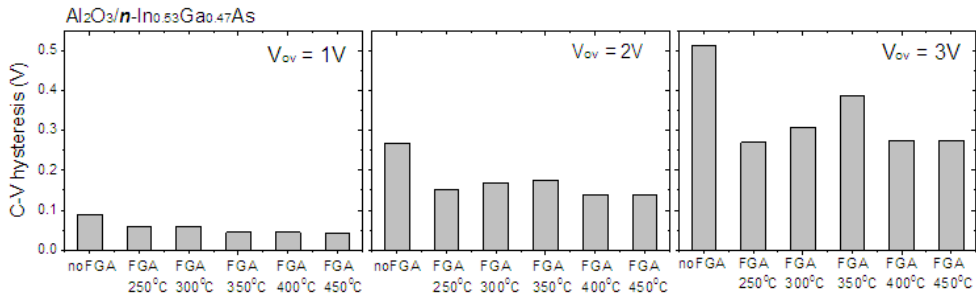


Figure 5.26: C-V hysteresis for $\text{Au/Ni/Al}_2\text{O}_3(8\text{nm})/\text{n-In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors at $V_{ov} = 1V$, $2V$ and $3V$.

For $\text{Au/Ni/Al}_2\text{O}_3(8\text{nm})/\text{p-In}_{0.53}\text{Ga}_{0.47}\text{As}$ shown in Figure 5.27, the slope of ΔV versus V_{ov} is almost the same for all the FGA conditions. γ -factors are shown in Figure 5.28 and ΔV extracted at $V_{\text{ov}} = 1\text{V}$, 2V and 3V is shown in Figure 5.29, which can be representative of the trend of C-V hysteresis at all V_{ov} values following all the FGA conditions due to the same γ -factors. In this case, neglecting FGA 400°C as discussed earlier, it can be concluded that FGA at $\geq 350^\circ\text{C}$ degrade the sample behavior by significantly increasing the C-V hysteresis, however FGA at 250°C doesn't have noticeable effect on C-V hysteresis compared to the no FGA sample and FGA 300°C only slightly increase ΔV .

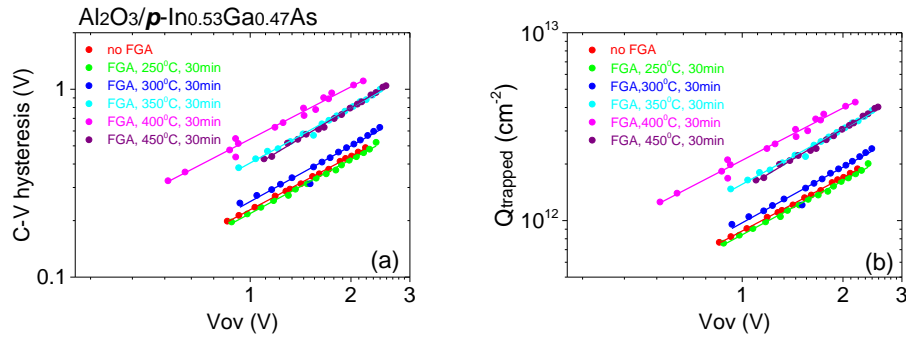


Figure 5.27: (a) C-V hysteresis and (b) the corresponding charge trapping density as a function of overdrive voltage for $\text{Au/Ni/Al}_2\text{O}_3(8\text{nm})/\text{p-In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors.

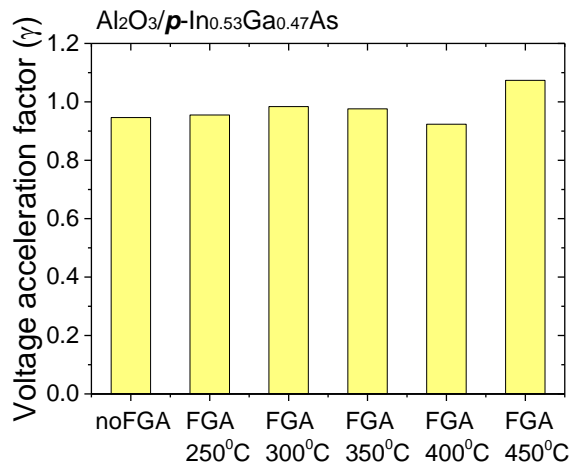


Figure 5.28: Voltage acceleration factor for $\text{Au/Ni/Al}_2\text{O}_3(8\text{nm})/\text{p-In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors.

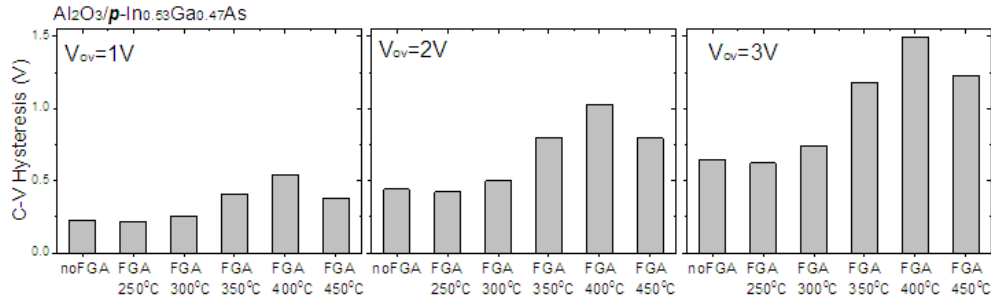


Figure 5.29: C-V hysteresis for Au/Ni/Al₂O₃(8nm)/p-In_{0.53}Ga_{0.47}As MOS capacitors at $V_{ov} = 1V, 2V$ and $3V$.

To conclude the effect of FGA on C-V hysteresis (or $Q_{trapped}$), $Q_{trapped}$ at $V_{ov} = 1V$ is plotted as a function of FGA condition for (a) HfO₂/n-In_{0.53}Ga_{0.47}As, (b) HfO₂/p-In_{0.53}Ga_{0.47}As, (c) Al₂O₃/n-In_{0.53}Ga_{0.47}As and (d) Al₂O₃/p-In_{0.53}Ga_{0.47}As MOS structures as shown in Figure 5.30. It is demonstrated that FGA 350⁰C is the most effective in reducing $Q_{trapped}$ for HfO₂/n-In_{0.53}Ga_{0.47}As MOS system at low V_{ov} . For HfO₂/p-In_{0.53}Ga_{0.47}As, the no FGA sample cannot reach strong accumulation; therefore it is impossible to conclude if FGA has any effect on $Q_{trapped}$. For Al₂O₃/In_{0.53}Ga_{0.47}As MOS system neglecting FGA 400⁰C, for n-In_{0.53}Ga_{0.47}As, FGA at all the temperatures under investigation reduce $Q_{trapped}$ compared to the no FGA sample and FGA $\geq 350^0C$ is the most effective in reducing $Q_{trapped}$. For Al₂O₃/p-In_{0.53}Ga_{0.47}As, FGA at relatively low temperatures (250⁰C and 300⁰C) almost have no effect on $Q_{trapped}$, however, FGA $\geq 350^0C$ increases $Q_{trapped}$.

In terms of the γ -factor, all the γ -factors extracted from the C-V hysteresis (or $Q_{trapped}$) versus V_{ov} for both HfO₂/In_{0.53}Ga_{0.47}As and Al₂O₃/In_{0.53}Ga_{0.47}As MOS capacitors under investigation is almost consistent with the reported γ -factor (~ 1.5) for Al₂O₃/In_{0.53}Ga_{0.47}As transistor, ascribed to a wide energy distribution of border traps when compared to high- k /Si MOS devices which have much larger γ -factor values (i.e. $\gamma=3$ for high- k /p-Si MOS and $\gamma=7.5$ for high- k /n-Si MOS) [13].

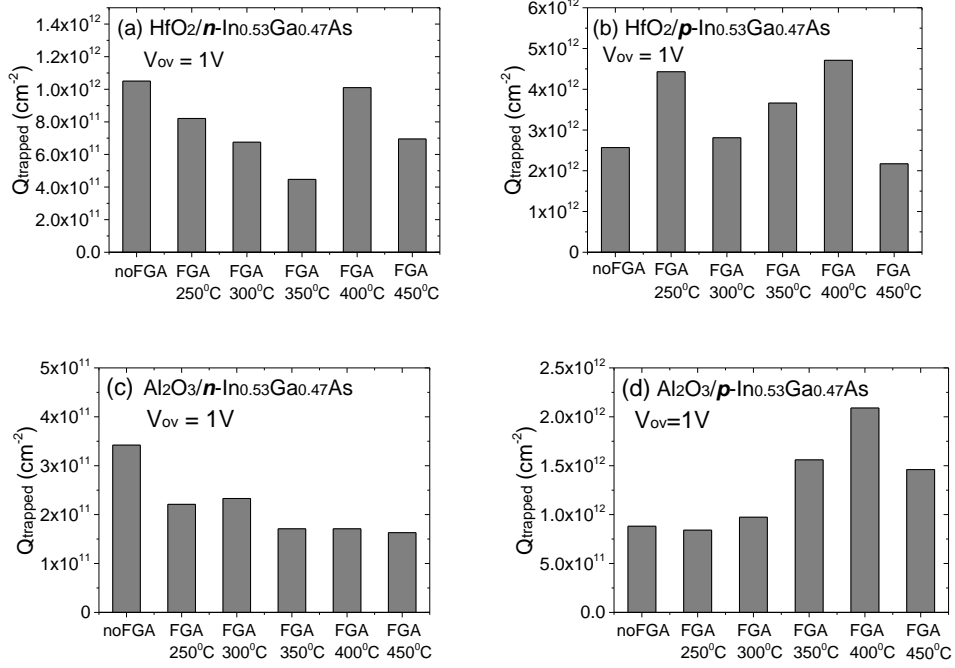


Figure 5.30: $Q_{trapped}$ (at $V_{ov}=1V$) versus FGA condition for Au/Ni gate over (a) $HfO_2(8nm)/n-In_{0.53}Ga_{0.47}As$, (b) $HfO_2(8nm)/p-In_{0.53}Ga_{0.47}As$, (c) $Al_2O_3(8nm)/n-In_{0.53}Ga_{0.47}As$ and (d) $Al_2O_3(8nm)/p-In_{0.53}Ga_{0.47}As$ MOS capacitors.

5.4 Effect of FGA and 10% $(NH_4)_2S$ on TiN/ Al_2O_3 /n-In_{0.53}Ga_{0.47}As MOS Systems

The effect of FGA (400⁰C, 5min) and the standard pre-ALD 10% $(NH_4)_2S$ surface passivation on the C-V hysteresis will be discussed in this section. The FGA at 400⁰C for 5min was performed in IMEC, and all the C-V hysteresis measurements presented in this section were carried out in IMEC. For the presented results in this section, the flatband voltage (V_{fb}) was determined by taking the 1st derivative of the upward C-V where the C-V was swept from inversion to accumulation and finding the peak value (i.e. the gate voltage where the maximum value of the C-V slope occurred) [15]. The capacitance equivalent thickness (CET in cm) was calculated using equation (5.1).

$$CET = \frac{3.9 \times \epsilon_0 \times Area}{C_{max}} \quad (5.1)$$

where the capacitance at $V_{fb}+1V$ was used for as the C_{max} (in F), ϵ_0 is the vacuum permittivity in F/cm and device area is in cm².

The trapping density (ΔN_{eff}) is calculated using equation (5.2).

$$\Delta N_{\text{eff}} = \frac{(3.9 \times \epsilon_0 / \text{CET}) \times \Delta V}{q} \quad (5.2)$$

where ΔV is the C-V hysteresis in V and q is the elementary charge in C.

The electric field across the oxide is estimated using equation (5.3).

$$E_{\text{ox}} = \frac{V_{\text{ov}}}{\text{CET}} \quad (5.3)$$

where V_{ov} is the overdrive voltage and $V_{\text{ov}} = |V_{\text{max}} - V_{\text{fb}}|$.

By plotting the x axis as V_{ov}/CET , which represents the oxide field during the stress, the sample results can be normalized for differences in the V_{fb} value for differing surface processing and samples with and without FGA (400°C, 5min).

C-V hysteresis as a function of overdrive voltage and the corresponding ΔN_{eff} as a function of oxide field for TiN/Al₂O₃(4nm)/n-In_{0.53}Ga_{0.47}As MOS capacitors are illustrated in Figure 5.31, showing that the 10% (NH₄)₂S surface passivation (SP) has very limited effect on the C-V hysteresis. However, the FGA (400°C, 5min) reduces the C-V hysteresis significantly. Figure 5.32 shows ΔN_{eff} (estimated at 3.5MV/cm using Figure 5.31(b)) and indicates that the trapping density is reduced by a factor of ~3 after the FGA (400°C, 5min). The best C-V hysteresis and trapping level is observed in the sample treated by both the SP and FGA (400°C, 5min).

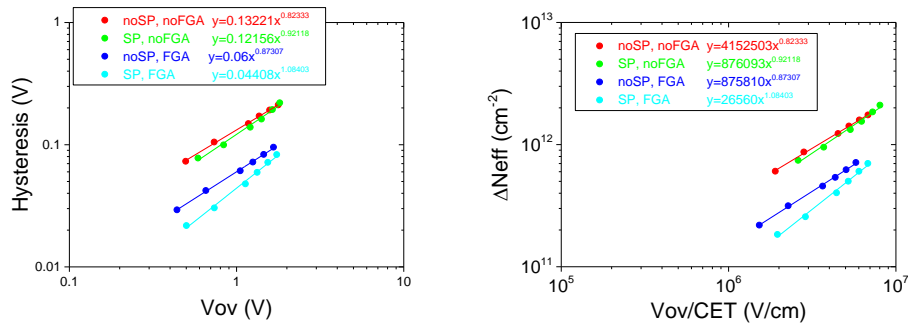


Figure 5.31: (a) C-V hysteresis as a function of overdrive voltage (V_{ov}) and (b) the corresponding trapping density (ΔN_{eff}) as a function of oxide field (V_{ov}/CET) for TiN/Al₂O₃(4nm)/n-In_{0.53}Ga_{0.47}As MOS capacitors.

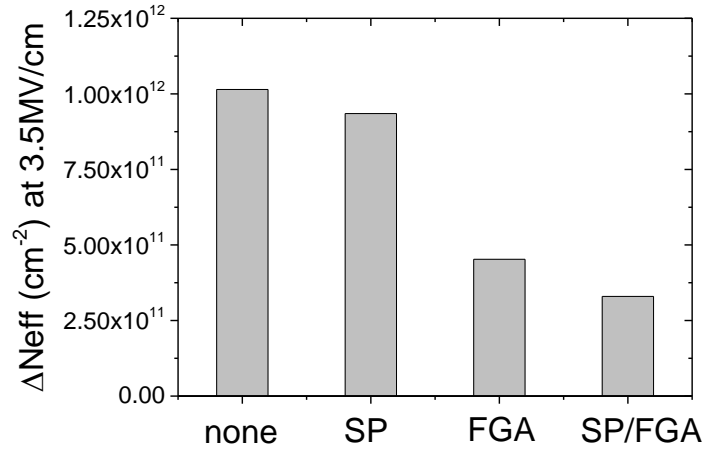


Figure 5.32: ΔN_{eff} (at 3.5MV/cm) for $\text{TiN}/\text{Al}_2\text{O}_3(4\text{nm})/\text{n-In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors.

5.5 Conclusions

In this chapter, a systematic study of the effect of FGA (5% H_2 / 95% N_2) at a series of temperatures (250⁰C, 300⁰C, 350⁰C, 400⁰C and 450⁰C) for 30min on the electrical characteristics is carried out on Au/Ni gate over both $\text{HfO}_2(8\text{nm})/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and $\text{Al}_2\text{O}_3(8\text{nm})/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors. It is shown that the gate leakage current increases significantly for samples treated with $\text{FGA} \geq 400^0\text{C}$ for all MOS structures except for $\text{Al}_2\text{O}_3/p\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ structure where an increase in leakage is only observed in FGA 400⁰C sample but not the FGA 450⁰C sample. It has been noted in the discussion that the Al_2O_3 samples (both $n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ and $p\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$) treated with FGA at 400⁰C exhibit non-regular behavior therefore for Al_2O_3 samples FGA 400⁰C is omitted in the discussion.

Multi-frequency C-V characteristics were investigated. It is observed that for $\text{HfO}_2/n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS structure FGA at all temperatures under study improve multi-frequency C-V responses in terms of accumulation frequency dispersion, C-V stretch-out and D_{it} responses in inversion. It is demonstrated for $\text{HfO}_2/n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ that the accumulation frequency dispersion goes through a valley with increasing FGA temperature where FGA at intermediate temperatures (300⁰C and 350⁰C) are the most effective in reducing accumulation frequency dispersion. For $\text{HfO}_2/p\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS

system, a significantly large level of accumulation frequency dispersion is observed prior to FGA. Multi-frequency C-V responses are only improved for FGA 250⁰C to 350⁰C and increasing FGA temperature (400⁰C and 450⁰C) degraded frequency dispersion indicating the movement of Fermi level is strongly restricted. For Al₂O₃/*n*-In_{0.53}Ga_{0.47}As MOS system, accumulation frequency dispersion is observed to decrease with increasing FGA temperature and C-V stretch-out is also improved following the FGA. The best C-V characteristics are observed for the sample treated with FGA 450⁰C, where the estimated D_{it} is $\sim 2.19 \times 10^{11} \text{cm}^{-2} \text{eV}^{-1}$, which is about an order of magnitude lower than the no FGA sample. For the case of Al₂O₃/*p*-In_{0.53}Ga_{0.47}As MOS system, there is no significant improvement in the accumulation frequency dispersion nor the C-V stretch-out following the FGA.

C-V hysteresis (or $Q_{trapped}$) is investigated as a function of overdrive voltage (V_{ov}). The slope, referred to as the voltage acceleration factor (γ), is also analyzed. It is shown that the γ -factor for HfO₂/*n*-In_{0.53}Ga_{0.47}As treated with FGA 300⁰C and 350⁰C are slightly improved when compared with other FGA conditions, resulting in reduced $Q_{trapped}$ at low V_{ov} (e.g. $V_{ov} = 1\text{V}$). The increase in γ -factor indicates that the corresponding FGA condition reduces the spread of the border trap defect energy levels, i.e. passivate the most extreme defect configurations. For the case of HfO₂/*p*-In_{0.53}Ga_{0.47}As, the sample prior to FGA have shown that the flatband cannot be reached therefore it is impossible to conclude if FGA has any effect on charge trapping. For Al₂O₃ samples, γ -factor changes slightly over different FGA conditions for both *n*-In_{0.53}Ga_{0.47}As and *p*-In_{0.53}Ga_{0.47}As samples therefore it is assumed that γ -factor remains constant. This indicates that FGA does not change the distribution of oxide traps. It is demonstrated that FGA at all temperature reduce $Q_{trapped}$ for Al₂O₃/*n*-In_{0.53}Ga_{0.47}As and for the case of Al₂O₃/*p*-In_{0.53}Ga_{0.47}As, FGA at 250⁰C and 300⁰C have negligible effect on $Q_{trapped}$, however, $\text{FGA} \geq 350^0\text{C}$ increases $Q_{trapped}$.

Another study based on the effect of both FGA (at 400⁰C for 5min) and the optimized 10% (NH₄)₂S surface passivation on C-V hysteresis for TiN/Al₂O₃(4nm)/*n*-In_{0.53}Ga_{0.47}As MOS capacitor is also performed. It has been shown that the (NH₄)₂S surface passivation has very limited effect on the C-V hysteresis and the FGA (400⁰C, 5min) reduces the C-V hysteresis significantly. The most reduced C-V hysteresis is observed in the sample treated with both FGA (400⁰C, 5min) and the 10% (NH₄)₂S surface passivation.

Bibliography

- [1] E. O'Connor, S. Monaghan, R. D. Long, A. O'Mahony, I. M. Povey, K. Cherkaoui, M. E. Pemble, G. Brammertz, M. Heyns, S. B. Newcomb, V. V. Afanas'ev, and P. K. Hurley, *Appl. Phys. Lett.* **94**, 102902 (2009).
- [2] B. Shin, J. R. Weber, R. D. Long, P. K. Hurley, C. G. Van de Walle, and P. C. McIntyre, *Appl. Phys. Lett.* **96**, 152908 (2010).
- [3] R. D. Long, B. Shin, S. Monaghan, K. Cherkaoui, J. Cagnon, S. Stemmer, P. C. McIntyre, and P. K. Hurley, *J. Electrochem. Soc.* **158**, G103 (2011).
- [4] V. Djara, K. Cherkaoui, M. Schmidt, S. Monaghan, E. O'Connor, I. M. Povey, D. O'Connell, M. E. Pemble, and P. K. Hurley, *IEEE Trans. Electron Devices* **59**(4), 1084–1090 (2012).
- [5] E. O'Connor, B. Brennan, V. Djara, K. Cherkaoui, S. Monaghan, S. B. Newcomb, R. Contreras, M. Milojevic, G. Hughes, M. E. Pemble, R. M. Wallace, and P. K. Hurley, *J. Appl. Phys.* **109**, 024101 (2011).
- [6] Y. Yuan, L. Wang, B. Yu, B. Shin, J. Ahn, P. C. McIntyre, P. M. Asbeck, M. J. W. Rodwell, and Y. Taur, *IEEE Electron Device Lett.* **32**(4), 485–487 (2011).
- [7] G. Brammertz, A. Alian, D. H.-C. Lin, M. Meuris, M. Caymax, and W.-E. Wang, *IEEE Trans. Electron Devices*, **58**(11), 3890–3897 (2011).
- [8] J. Wu, K. Jansson, A. S. Babadi, M. Berg, E. Lind, and L.-E. Wernersson, *IEEE Trans. Electron Devices*, **63**(2), 584–589 (2016).
- [9] V. Djara, T. P. O'Regan, K. Cherkaoui, M. Schmidt, S. Monaghan, É. O'Connor, I. M. Povey, D. O'Connell, M. E. Pemble, and P. K. Hurley, *Microelectronic Engineering* **109**, 182 (2013).
- [10] G. Brammertz, H. C. Lin, M. Caymax, M. Meuris, M. Heyns, and M. Passlack, *Appl. Phys. Lett.* **95**, 202109 (2009).
- [11] P. K. Hurley, E. O'Connor, S. Monaghan, R. D. Long, A. O'Mahony, I. M. Povey, K. Cherkaoui, J. MacHale, A. J. Quinn, and G. Brammertz, M. Heyns, S. B. Newcomb, V. V. Afanas'ev, A. M. Sonnet, R. V. Galatage, M. N. Jivani, E. M. Vogel, R. M. Wallace and M. E. Pemble, *ECS Trans.* **25**(6), 113 (2009).

- [12] S. Monaghan, E. O'Connor, R. Rios, F. Ferdousi, L. Floyd, E. Ryan, K. Cherkaoui, I. M. Povey, K. J. Kuhn and P. K. Hurley , IEEE Trans. Electron Devices, **61**(12), 4176–4185 (2014).
- [13] J. Franco, A. Alian, B. Kaczer, D. Lin, T. Ivanov, A. Pourghaderi, K. Martens, Y. Mols, D. Zhou, N. Waldron, S. Sioncke, T. Kauerauf, N. Collaert, A. Thean, M. Heyns, and G. Groeseneken, Tech. Dig. -Int. Reliab. Phys. Symp. 2014, 6A.2.1.
- [14] A. Vais, J. Franco, H-C Lin, N. Collaert, A. Mocuta. K. De Meyer, and A. Thean, Appl. Phys. Lett. **107**, 233504 (2015).
- [15] R. Winter, J. Ahn, P. C. McIntyre and M. Eizenberg, J. Vac. Sci. Technol. B **31**, 030604 (2013).

Chapter 6: A Combined Capacitance-Voltage and Hard X-ray Photoelectron Spectroscopy Characterization of Metal/ Al_2O_3 / $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS Structures

6.1 Introduction

As is evident from previous chapters in the thesis, electrically active interface states are present at the oxide/III-V interface which can restrict efficient III-V surface Fermi level movement. From chapters considering the case of the high- k /III-V MOS system, there is a wide range of interface state concentrations (interface state density distribution as a function of energy in the III-V bandgap, i.e. $D_{it}(E)$) reported for nominally similar structures [1-5]. One of the main issues associated with the accurate extraction of $D_{it}(E)$ for the high- k /III-V MOS system is the question of how each gate voltage (V_g) is related to the corresponding surface Fermi level position (E_f) relative to the valence band edge (E_v). For a $D_{it}(E)$, which changes density exponentially with $E_f - E_v$, this is clearly a potential source of error and variation between research groups. Moreover, the relationship of $E_f - E_v$ to V_g is further complicated in the case of high D_{it} and for MOS systems where the semiconductor has a low conduction band density of states as in the case of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$. This combined effect results in difficulty with the accurate extraction of the oxide capacitance, which is required when relating V_g to a corresponding $E_f - E_v$. The objective of the studies reported in this chapter of the PhD are focussed on a route to provide more certainty on $D_{it}(E)$

extractions and also bridge the gap between interface chemistry and electrical properties at a buried interface.

In this chapter, a combined C-V and hard x-ray photoelectron spectroscopy (HAXPES) study in MOS capacitors fabricated using both high (Ni 5.01eV) and low (Al 4.08eV) work function metal gates [6] on ALD deposited Al_2O_3 on $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ is investigated. The main objective of this study is to compare the surface Fermi level positions (at room temperature) analyzed by C-V characteristics at zero gate bias ($V_g=0\text{V}$) and HAXPES measurements without applying a gate bias, and furthermore, to investigate the Fermi level movement at the $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface and the change in potential drop across the dielectric layer, resulting from the deposition of metals with different work functions. Experimental details and theories of determination of E_f-E_v using C-V and HAXPES techniques will be discussed in section 6.2. Results and analysis will be presented in section 6.3 and conclusion of this work is in section 6.4.

As the use of combined C-V and HAXPES measurements to determine surface potentials is a new area of research, the initial study was performed on MOS structures formed on thermally oxidized silicon, to provide a baseline for a system which is relatively well understood. Following this initial study, the combined technique was applied to the case of the GaAs MOS system, which is known to exhibit very high densities of interface states, and for oxides formed by ALD, the surface Fermi Level is typically pinned [7]. These two system represented cases of low (SiO_2/Si) and high ($\text{Al}_2\text{O}_3/\text{GaAs}$) interface state density values and were the basis for the study of the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS structures reported in this chapter. These results were published in [8] for the SiO_2 MOS system and [9] for the $\text{Al}_2\text{O}_3/\text{GaAs}$ system, and the papers are included in Appendix VI.

6.2 Experiments and Theories

6.2.1 Experimental Samples

The samples studied in this work were heavily *n*-doped (S at $2 \times 10^{18} \text{cm}^{-3}$) and heavily *p*-doped (Zn at $2 \times 10^{18} \text{cm}^{-3}$) InP(100) substrates with $2 \mu\text{m}$ *n*-type (S at $4 \times 10^{17} \text{cm}^{-3}$) and *p*-type (Zn at $4 \times 10^{17} \text{cm}^{-3}$) $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ epitaxial layers, respectively, grown by metal organic vapour phase epitaxy (MOVPE). The $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ surfaces were immersed in a $(\text{NH}_4)_2\text{S}$ solution (10% in deionized H_2O) for 20min at room temperature (295K) prior to ALD. Samples were then introduced to the ALD chamber load lock after the removal from the 10% $(\text{NH}_4)_2\text{S}$ surface passivation solution within 3min [10]. The Al_2O_3 dielectric layer, which had a nominal thickness of 8nm, was deposited by ALD at 300°C using trimethylaluminum (TMA) $\text{Al}(\text{CH}_3)_3$ and H_2O as precursors.

For C-V analysis, either Al(160nm) or Ni(70nm)/Au(90nm) were used as the metal gate electrodes, which were formed by electron beam evaporation and a lift-off process. For HAXPES analysis, one *n*-type and one *p*-type $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ sample were left without a metal gate. The other HAXPES samples were capped with either Al(5nm) or Ni(5nm) blanket films formed by electron beam evaporation. The full sample details are in Table 6.1.

Table 6.1 Sample details for combined C-V and HAXPES study

Sample	oxide	metal
<i>n</i> - & <i>p</i> - $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ (C-V)	Al_2O_3 (8nm)	Al (160nm)
<i>n</i> - & <i>p</i> - $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ (C-V)	Al_2O_3 (8nm)	Ni/Au (70nm/90nm)
<i>n</i> - & <i>p</i> - $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ (HAXPES)	Al_2O_3 (8nm)	Al (5nm)
<i>n</i> - & <i>p</i> - $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ (HAXPES)	Al_2O_3 (8nm)	Ni (5nm)
<i>n</i> - & <i>p</i> - $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ (HAXPES)	Al_2O_3 (8nm)	no metal

6.2.2 Theories of C-V and HAXPES in Determining Fermi Level

Position

C-V analysis

The C-V measurements were recorded using a C-V enabled B1500a semiconductor analyzer following an open correction and performed in a probe station in a dry air, dark environment. The C-V characteristics measured at both room temperature and -50°C were compared in order to rule out the possible contribution of an interface state capacitance to the overall measured capacitance of the MOS capacitors at room temperature. The oxide capacitance and flatband capacitance used for C-V analysis are calculated using a dielectric constant value of 8.6 for Al_2O_3 [11] and accurate oxide thicknesses were obtained from high-resolution cross-sectional transmission electron microscopy (HR-TEM). On the premise that a true high frequency C-V can be obtained, interface state capacitance associated capacitance (C_{it}) is taken out from the equivalent circuit of MOS capacitor with interface states. The differential capacitance (C_s) of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ can be determined using the measured capacitance (C_m) and oxide capacitance (C_{ox}) (equation (6.1)). With known C_s , the surface potential (Ψ_s) is determined (equation (6.2)) and so is the Fermi level position at the $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface (equation (6.3)).

$$\frac{1}{C_s} = \frac{1}{C_m} - \frac{1}{C_{ox}} \quad (6.1)$$

$$|\Psi_s| = \frac{qN_{\text{doping}}w^2}{2\epsilon_s\epsilon_0} \quad (6.2)$$

where w is the depletion layer width ($w = \epsilon_s\epsilon_0/C_s$) and ϵ_s is the relative permittivity of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$.

$$\text{For } n\text{-type in depletion, } E_f - E_V = (E_i - E_V) + |\Phi_B| - |\Psi_s| \quad (6.3a)$$

$$\text{For } p\text{-type in depletion, } E_f - E_V = (E_i - E_V) - |\Phi_B| + |\Psi_s| \quad (6.3b)$$

HAXPES technique

HAXPES is emerging as a technique that has the capability of providing chemical and electronic information on much larger depth scales than conventional x-ray photoelectron spectroscopy [8, 9, 12, 13]. HAXPES measurements discussed in this thesis were carried out on the X24A

beamline at the National Synchrotron Light Source (NSLS) at Brookhaven National laboratory (BNL). A double Si (111) crystal monochromator allowed for photon energy selection in the range of 2.1–5.0keV. An electron energy analyzer was operated at a pass energy of 200eV giving an overall instrumental energy resolution of ~0.52eV at the photon energy of 4150eV. Samples were fixed on a grounded Al sample holder with stainless steel clips, which connected the front of the samples to the sample holder. In order to ensure correct energy calibration throughout the experiment, metallic Ni Fermi edge reference spectra were acquired immediately before and after the acquisition of the Al₂O₃ and In_{0.53}Ga_{0.47}As substrate core level peaks. The resultant error associated with this photon energy correction procedure is estimated to be no more than ±50meV.

The calculated depletion region width for the $4 \times 10^{17} \text{cm}^{-3}$ doped In_{0.53}Ga_{0.47}As substrate is 51nm and the total sampling depth of the HAXPES measurements for the metal capped samples is estimated to be ~23nm at 4150eV [14] for the substrate Ga 2p and As 2p which have kinetic energies of 3033eV and 2827eV, respectively [15]. This means that for a 5nm thick metal capping layer and an 8nm Al₂O₃ layer, the sampling depth (λ) into the In_{0.53}Ga_{0.47}As is ~10nm (see Figure 6.1). Therefore, the acquired peaks directly reflect the binding energy (BE) of the core levels with respect to the Fermi level near the top of the depletion region adjacent to the dielectric interface. As the energy difference between the core level and the valence band edge is a constant (see Figure 6.1), any observed shift in BE equals the shift in the Fermi level position in the bandgap near the oxide/semiconductor interface. All core level peaks were curve fitted in order to increase the accuracy of locating the peak centre positions.

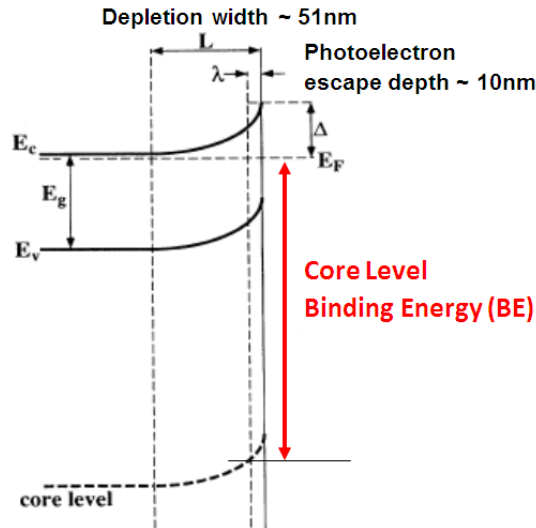


Figure 6.1: Illustration of HAXPES concept. The difference between core level energy and valence band edge is a constant. Therefore the shift in BE equals to the movement of Fermi level position near the oxide/semiconductor interface.

6.3 Determination of Fermi Level Position Based on Combined C-V and HAXPES Analysis

The C-V characteristics at 1MHz and 295K for Al(160nm) or Au(90nm)/Ni(70nm) metal gate MOS capacitors are shown in Figures 6.2(a) and 6.2(b) for $\text{Al}_2\text{O}_3/n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ and $\text{Al}_2\text{O}_3/p\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$, respectively. If interface states can respond at these measurement conditions, the measured capacitance (C_m) will have a contribution from interface states (C_{it}), which is frequency and temperature dependent, and can be suppressed at a higher frequency and/or lower temperature [16-18]. This will especially affect the C-V responses in terms of frequency dispersion in the accumulation region at different temperatures. Therefore, a significantly lower level of accumulation frequency dispersion and a decrease in the 1MHz C_m are expected at a lower temperature when compared to the measurements at room temperature. It is believed that a true high frequency C-V is achieved at 1MHz and room temperature as the multi-frequency (1kHz to 1MHz) and 1MHz C-V measured at room temperature have very similar characteristics when compared to the C-V measured at -50°C for the $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors under investigation. Based on this observation we take the 1MHz

room temperature response to be an accurate representation of a high frequency C-V for the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ structures examined in this study.

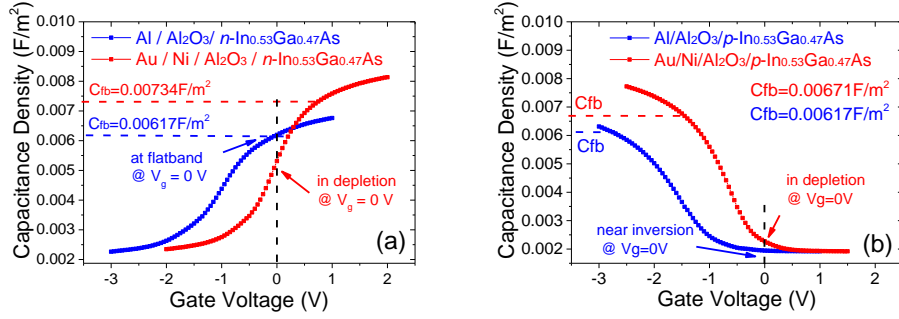


Figure 6.2: C-V responses at 1MHz and 295K for Al gate and Au/Ni gate over (a) $\text{Al}_2\text{O}_3/\text{n-In}_{0.53}\text{Ga}_{0.47}\text{As}$ and (b) $\text{Al}_2\text{O}_3/\text{p-In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors.

As observed in the TEM images in Figure 6.3, a thicker Al_2O_3 film is formed under the Al gate due to a more reactive Al/ Al_2O_3 interface compared to a non-reactive Ni/ Al_2O_3 interface. This is consistent with the lower oxide capacitance and thus the lower measured capacitance in accumulation for the Al gate samples as observed in Figures 6.2(a) and 6.2(b). Using the oxide thickness measured by HR-TEM in Figure 6.3, the oxide capacitance (C_{ox}) is calculated and used to determine the flatband capacitance (C_{fb}). Furthermore, the calculated C_{fb} can be used to determine the region of operation of the MOS capacitor and to establish if at $V_g=0\text{V}$, the surface Fermi level position can be determined using the depletion capacitance. From the C-V for $\text{n-In}_{0.53}\text{Ga}_{0.47}\text{As}$ in Figure 6.2(a), the measured capacitance for the Ni gate sample is below the calculated C_{fb} ($\sim 0.00734\text{F/m}^2$) and is thus operating in depletion at $V_g=0\text{V}$. The corresponding $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ depletion capacitance (C_s) can be calculated using the measured capacitance C_m ($C_{\text{it}}=0$) and an oxide capacitance value of $1.27 \times 10^{-6}\text{F/cm}^2$. The C_s value can be used to calculate the surface Fermi level position with respect to valence band maximum (VBM) energy level (see section 6.2) and for Ni gate $\text{n-In}_{0.53}\text{Ga}_{0.47}\text{As}$ yielding a value of $\sim 0.71\text{eV}$ above VBM.

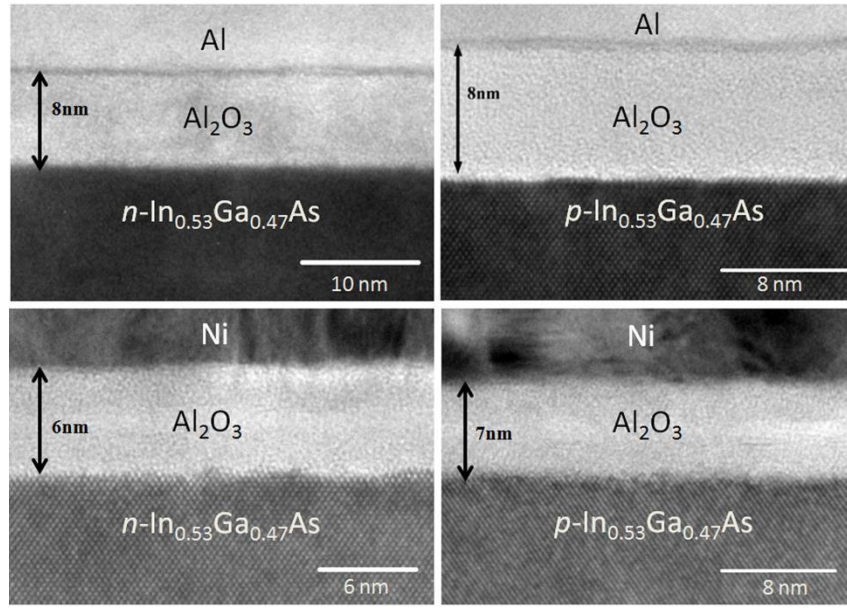


Figure 6.3: Transmission electron microscopy images of the MOS capacitors under investigation. Note that there is no clear evidence of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ native oxides at the $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface, which is consistent with the $(\text{NH}_4)_2\text{S}$ treatment prior to the ALD process [10] and the reported “self-cleaning” process of ALD of Al_2O_3 [19, 20].

For the Al gate $n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ sample shown in Figure 6.2(a), the C_m at $V_g=0\text{V}$ approximately equals the C_{fb} value ($\sim 0.00617\text{F/m}^2$), which indicates that the sample is near the flatband condition and its surface potential is approximately zero at $V_g=0\text{V}$. Thus the Fermi level position for this sample is $\sim 0.76\text{eV}$ above the VBM at the flatband condition for Al gate n -type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$. From the C-V for Ni gate and Al gate over $p\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ shown in Figure 6.2(b), both samples are operating in depletion region at $V_g=0\text{V}$. Using the same method of surface Fermi level calculation for Ni gate over $n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ (Figure 6.2(a)), the Fermi level is determined to be $\sim 0.55\text{eV}$ and $\sim 0.73\text{eV}$ above VBM with Ni and Al gates, respectively.

Figure 6.4 shows the HAXPES As 2p core levels acquired at 4150eV photon energy for both n - and $p\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ with an Al_2O_3 dielectric layer with and without the presence of the metal gate. For the unmetallised samples, the binding energy position for the $p\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ peaks was found to be $\sim 0.28\text{eV}$ lower than the $n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ substrate consistent with the p -type

sample Fermi level residing closer to the VBM. The difference is however less than the expected difference of 0.68eV, which is calculated from the difference in Fermi level position for n - and p - $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ for a doping level of $4 \times 10^{17} \text{cm}^{-3}$ [16, 17], indicating that there is band bending present at the $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface prior to metal contact.

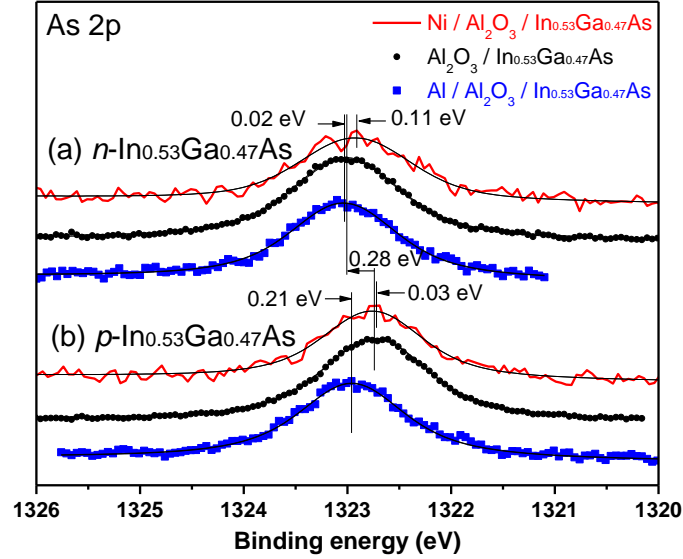


Figure 6.4: Normalised and fitted As 2p core level spectra acquired at a photon energy of 4150eV for the uncapped $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ (black), Ni(5nm) capped (red), and Al(5nm) capped (blue) $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ samples, showing the shifts in the core level BE after metal for (a) n - $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, and (b) p - $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ substrates. The energy separation between the n - and p - $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ without metal gates is 0.28eV. The biggest BE shift occurs in the p - $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ sample with an Al gate. This is consistent with lower D_{it} distribution in the upper bandgap which allows for a more efficient Fermi level movement.

In order to establish the absolute position of the Fermi level in the bandgap with respect to the valence band edge, valence band spectra were acquired at the same photon energy for the unmetallized $\text{Al}_2\text{O}_3/n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ sample. An extrapolation of the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ valence band to a zero signal intensity yields the approximate position of the valence band edge [21]. Although more accurate methods have been recently employed [9, 22], this method is

sufficient to provide an accuracy of approximately 0.1eV in these studies. Reference spectra of the nickel metallic edge were subsequently acquired in order to establish the Fermi level position. The value of $E_F - E_v$ is thus determined for the $\text{Al}_2\text{O}_3/n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ sample with no metal gate. On the same sample, the As 2p spectra are recorded (see Figure 6.4). These measurements provide the necessary reference for all the other samples to allow the value of $E_F - E_v$ to be evaluated. The energy separation between the core level and the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ valence band maxima is a constant; therefore, any changes in the As 2p spectra in Figure 6.4 are a consequence of changes in $E_F - E_v$. From the valence band spectra of the uncapped $\text{Al}_2\text{O}_3/n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ sample (not shown), the Fermi level is 0.67eV above the VBM and the equivalent measurement for the p -type Fermi level position is 0.39eV above the VBM. Therefore, the Fermi level is $\sim 0.09\text{eV}$ below flatband position for $n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ and is $\sim 0.31\text{eV}$ above flatband position (i.e., near mid-gap) for the $p\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$, indicating that the $n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ surface is slightly depleted and the $p\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ surface is strongly depleted.

Figures 6.5(a) and 6.5(b) schematically illustrates the band bending occurring for the unmetallised samples and the respective Fermi level positions (E_F) determined by HAXPES. The depletion of both the n - and p -type surface cannot be explained by one net oxide charge type. Therefore, the band bending occurring at the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ surface in the absence of metal gates is attributed to a combination of fixed charge in the Al_2O_3 layer and the interface states with energy levels within the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ bandgap, which deplete both the n -type and p -type surface. Based on the work by Long *et al* [23] the fixed oxide charge in ALD deposited Al_2O_3 is comprised of negative interface fixed charge that exists near the $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface and positive fixed charge distributed through the bulk of Al_2O_3 . For a relatively thin oxide of 8nm, the net fixed oxide charge (Q_f) could be negative as discussed in [23]. In addition, Ref [1, 23, 24] have reported the evidence that the net interface states type for Al_2O_3 on $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ is donor type (+/0). If this is the case, for an n -type sample at flatband where the E_F is close to conduction band edge and the interface state energy levels in the bandgap are

occupied, the interface defects (Q_{it}) are neutral. The combination of negative fixed charge Q_f and neutral Q_{it} is a negative charge, which slightly depletes the n -type surface as shown in Figure 6.5(a). For a p -type sample at flatband where E_f is close to valence band edge, the donor-type interface defects have a net associated positive charge as their energy levels in the bandgap are empty. The positively charged interface states plus the negatively charged Q_f can result in the depletion of p -type surface as shown in Figure 6.5(b) if $|Q_{it}| > |Q_f|$. Confirming the sign of Q_f and Q_{it} requires an Al_2O_3 thickness series as described in [23], which is beyond the scope of this work.

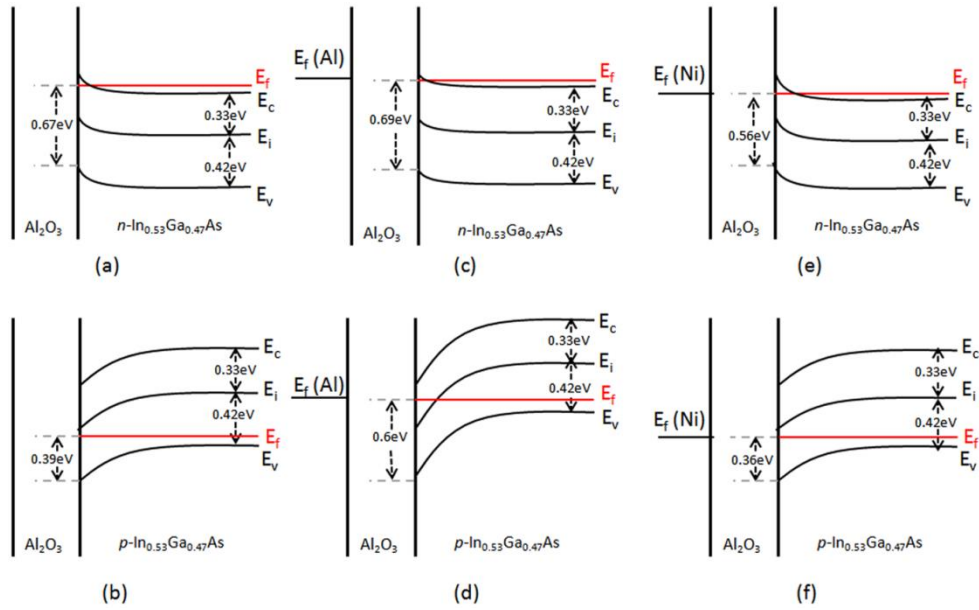


Figure 6.5: Band diagrams of (a) unmetallized $Al_2O_3/n-In_{0.53}Ga_{0.47}As$, (b) unmetallized $Al_2O_3/p-In_{0.53}Ga_{0.47}As$, (c) $Al_2O_3/n-In_{0.53}Ga_{0.47}As$ following Al deposition, (d) $Al_2O_3/p-In_{0.53}Ga_{0.47}As$ following Al deposition, (e) $Al_2O_3/n-In_{0.53}Ga_{0.47}As$ following Ni deposition, and (f) $Al_2O_3/p-In_{0.53}Ga_{0.47}As$ following Ni deposition MOS capacitors. The band bending occurring in the absence of a metal contact shown in (a) and (b) is due to a combined effect of fixed oxide charges and interface states. E_f represents the Fermi level position, E_c represents the conduction band edge, E_v represents the valence band edge and E_i represents the $In_{0.53}Ga_{0.47}As$ intrinsic Fermi level. The surface E_f-E_v values shown in this figure are determined from HAXPES.

In order to determine whether the band bending displayed at the interface reflects Fermi level pinning, both high (Ni) and low (Al) work function metals of 5nm in thickness were deposited on the dielectric. By ensuring electrical contact between the metal overlayer and the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ substrate, Fermi level equalisation across the MOS structure resulting from the differences in work functions occurs. If the Fermi level at the $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface is free to move, it would be expected to align with the metal Fermi level, resulting in an increase in BE with the low work function Al contact and a reduction in BE with the high work function Ni contact for both the n - and p - $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$. HAXPES measurements in Figure 6.4 show that, for the p - $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ sample, the core level peaks shifts by 0.21eV, and for the n - $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ sample, the peaks shifts by 0.02eV, both to higher BE, following the deposition of Al contact. Following the deposition of Ni contact, the peak positions shift 0.11eV for n - $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and 0.03eV for p - $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ to lower BE. The directions of all the BE shifts observed in the HAXPES spectra are consistent with the differences in the Fermi level positions for the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ substrates and metals. It should be noted that the small shifts of 0.02eV and 0.03eV, measured for the Al on n - $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and Ni on p - $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ respectively, are within the experimental error ($\pm 50\text{meV}$) of this technique; therefore, these shifts are almost negligible. The changes in $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ surface Fermi level when the metal contacts are present can be visualized using the schematic band diagrams and the Fermi levels presented in Figures 6.5(c)~(f). The corresponding Fermi level positions in the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ bandgap following either Al or Ni deposition are calculated from the HAXPES to be 0.69eV above VBM for the Al gate, and 0.56eV above VBM for Ni gate, over n - $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$. Both of these Fermi level positions are in general agreement with the C-V measurements at $V_g=0\text{V}$ shown in Figure 6.2(a) where the sample is in the near flatband condition for the Al gate and in depletion for the Ni gate. For the HAXPES p - $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ samples, the Fermi levels are determined to be 0.6eV above VBM with the Al gate and 0.36eV above VBM with the Ni gate, which are consistent with the C-V measurements at $V_g=0\text{V}$ in Figure 6.2(b) where both the samples are in

depletion with the Al gate sample being more depleted (near inversion) than the Ni gate sample.

In the HAXPES measurements, any large degree of band bending at the $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface may lead to an error in the surface Fermi level measurement, as HAXPES has a sampling depth into the substrate of $\sim 10\text{nm}$ so the Fermi level is being measured up to 10 nm below its surface position. In order to assess the magnitude of this error in determining the Fermi level position from the HAXPES measurement, a simulation of the band bending for $4 \times 10^{17}\text{cm}^{-3}$ doped $p\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ resulting from a 0.31eV surface potential was performed by numerically solving Poisson's equation.

The resulting band bending diagram (not shown) indicates that for a sampling depth into the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ substrate of $\sim 10\text{nm}$, the error in determining the VBM position is a maximum of 0.1eV. However, due to the exponential fall off in the weighting of the photoemitted electron contribution with depth, the actual error will be less than this value. This error can thus be taken into account when comparing the results of the approximate Fermi level position of each sample in the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ bandgap. A comparison between the Fermi level positions at the $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface derived from C-V analysis at $V_g=0\text{V}$ and the HAXPES measurements shown in Table 6.2 displays a reasonable agreement is achieved between the two techniques. The difference between the Fermi level position of Al and Ni obtained from C-V analysis are also consistent with that determined by HAXPES measurements. The difference between the C-V and HAXPES values for E_F-E_v are in the range of 0.1~0.2eV. This is comparable to the results obtained in the case of the $\text{Al}_2\text{O}_3/\text{GaAs}$ MOS system [9], but in the case of the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, this error represents a larger percentage of the semiconductor energy gap.

Table 6.2 Surface Fermi level positions obtained from C-V analysis at $V_g=0V$ and HAXPES measurements for uncapped, Al gate and Ni gate $Al_2O_3/In_{0.53}Ga_{0.47}As$ samples

Sample	$E_f - E_v$ (uncapped)	$E_f - E_v$ (Al gate)	$E_f - E_v$ (Ni gate)	ΔE_f (Al-Ni shift)
<i>n</i> -type (C-V)	N/a	0.76eV	0.71eV	0.05eV
<i>n</i> -type (HAXPES)	0.57→0.67eV	0.59→0.69eV	0.46→0.56eV	0.03→0.23eV
<i>p</i> -type (C-V)	N/a	0.73eV	0.55eV	0.18eV
<i>p</i> -type (HAXPES)	0.39→0.49eV	0.6→0.7eV	0.36→0.46eV	0.14→0.34eV

Further insight into the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface properties can be obtained from the HAXPES measurements in relation to the extent of the Fermi level movements at $In_{0.53}Ga_{0.47}As$ surface when a metal layer is deposited. Following the deposition of the Al gate, the surface Fermi level position of *n*- $In_{0.53}Ga_{0.47}As$ moves towards the conduction band edge. For the *p*- $In_{0.53}Ga_{0.47}As$ following Al deposition, the Fermi level moves towards conduction band edge residing slightly below the conduction band minimum. These experimental observations confirm the ability of the Fermi level in the $In_{0.53}Ga_{0.47}As$ bandgap to move towards the conduction band edge attempting to align with the Al Fermi level (see Figure 6.5). The fact that the surface Fermi level does not move significantly into the low density of states $In_{0.53}Ga_{0.47}As$ conduction band is also consistent with the reported high interface state density located within the $In_{0.53}Ga_{0.47}As$ conduction band where the Fermi level can be strongly pinned at energies above E_c [2, 25]. When the Ni gate is in contact, the $In_{0.53}Ga_{0.47}As$ Fermi level movement is more restricted. The inability to move the *n*- $In_{0.53}Ga_{0.47}As$ Fermi level to the lower bandgap and the slight Fermi level movement of only 0.03eV towards VBM for the *p*- $In_{0.53}Ga_{0.47}As$ suggest a peak D_{it} distribution (see Figure 6.6 [5]) where the density increases in the lower half of the bandgap, consistent with previous publications [26-28].

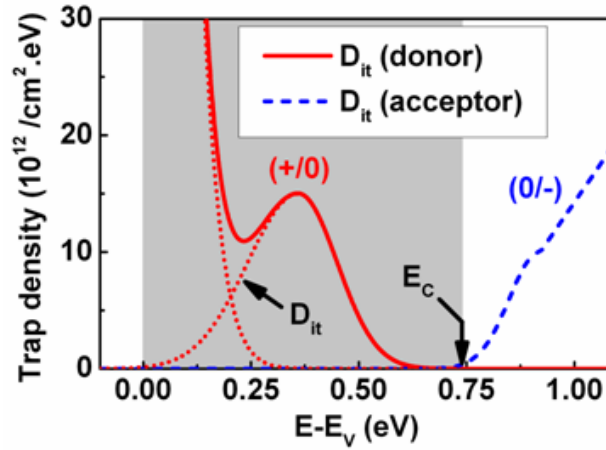


Figure 6.6: $D_{it}(E)$ for $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOS transistor. Source of Figure 6.6: V. Djara et al [5].

Fermi level alignment between the metal and the $In_{0.53}Ga_{0.47}As$ is achieved by not only the movement of $In_{0.53}Ga_{0.47}As$ Fermi level but also a change in the potential drop across the oxide layer. The change in the oxide potential following metal deposition will result in a binding energy shift of the associated Al 1s dielectric core levels, and the total potential drop across the oxide will result in an energy broadening of the peak [8, 9, 12]. Note that the shift resulting from Fermi level movement in the bulk $In_{0.53}Ga_{0.47}As$ is also present in the oxide core level, so any shift in the oxide peaks is a combination of the $In_{0.53}Ga_{0.47}As$ Fermi level movement and the change in the potential difference across the oxide. Based on the difference in metal and $In_{0.53}Ga_{0.47}As$ Fermi levels, the change in the Al 1s oxide binding energies would be expected to be more apparent in the p -type sample than in the n -type with Al as the metal gate, and more apparent in the n -type sample than in the p -type with Ni as metal gate. Figure 6.7 shows the changes in binding energy of the Al 1s oxide peak (at 1562eV) for the n - and p - $In_{0.53}Ga_{0.47}As$ substrate resulting from metal deposition.

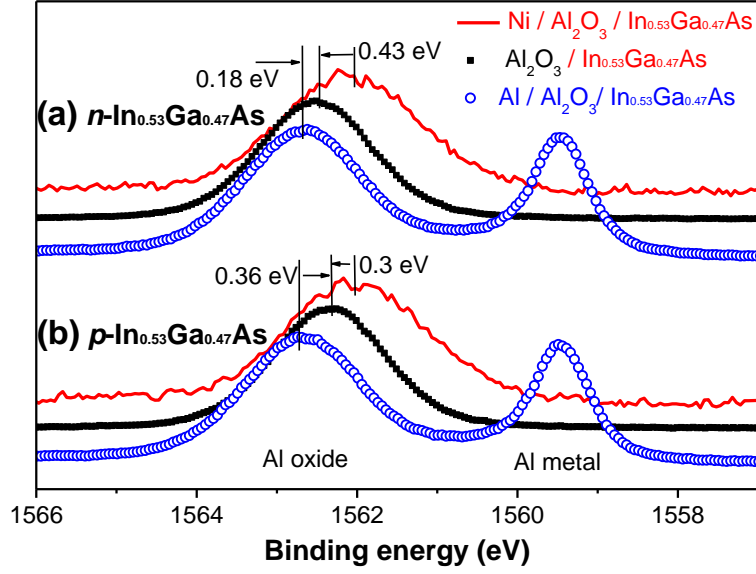


Figure 6.7: Al 1s spectra showing BE shift due to the changes in the potential across the Al_2O_3 layer caused by different work function metals and also the Fermi level movement in the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ for (a) $n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ and (b) $p\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$. The presence of a metallic Al 1s signal at $\sim 1559.5\text{eV}$ binding energy originates from the metal cap.

For $n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$, the deposition of the low work function Al only results in a small increase in the Al 1s peak binding energy in the Al_2O_3 ($\sim 0.18\text{eV}$), while for the $p\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ the deposition of Al results in a more significant increase in the binding energy ($\sim 0.36\text{eV}$) reflecting the larger Fermi level difference between $p\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ and Al gate. For $n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$, the deposition of Ni results in a decrease in the Al 1s peak binding energy ($\sim 0.43\text{eV}$), while for the $p\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ the deposition of high work function Ni results in a lower decrease in the binding energy ($\sim 0.3\text{eV}$), consistent with the larger Fermi level difference between $n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ and Ni compared to the case of $p\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$. All of these changes are consistent with the expected shifts and polarity of the band bending in the dielectric layer caused by the low and high work function metals.

The Al 1s peak widths for the metal capped samples broaden when compared to the samples without metal gates reflecting the gradient in the potential

across the dielectric layer. The change in the Al 1s binding energy of 0.18eV measured for the Al gate on *n*-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ sample results in broadening of 0.09eV (compared to the no metal gate sample) while a full width half maximum (FWHM) increase of 0.62eV is measured for Ni on *n*-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ sample. This infers a larger potential drop across the Al_2O_3 layer for the Ni *n*-type compared to the Al *n*-type samples. In the case of the *p*-type sample, a negligible difference in FWHM was measured for the Al contact, but a 0.46eV FWHM increase was found for the Ni capped sample, indicating a larger potential drop across the Al_2O_3 layer for the Ni capped *p*-type sample.

6.4 Conclusions

In summary, C-V analysis and HAXPES measurements have been made on metal/ Al_2O_3 / $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors with both high (Ni) and low (Al) work function metal gates. The HAXPES measurements reveal the presence of band bending prior to metal deposition, resulting from a combination of fixed oxide charges and possible donor-type interface states. Following the deposition of metal, the substrate core level BE shift in the expected directions. A reasonable agreement in Fermi level positions for the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS structures is obtained between C-V analysis and HAXPES measurements at zero gate bias. This combined C-V and HAXPES study provides more certainty on $D_{it}(E)$ extractions and also helps to bridge the gap between interface chemistry and electrical properties at a buried interface. The results point to a restricted Fermi level movement due to Al_2O_3 / $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface states and also suggest a higher interface state density in the lower half of the bandgap. There is a shift in binding energy of the oxide core levels following metal deposition, which is caused by the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ surface Fermi level movement and a change in the potential drop across the Al_2O_3 layer, and the shifts are in the expected directions. The broadening of the oxide peak widths indicates a higher potential drop across the Al_2O_3 layer with Ni gate than that with Al gate.

Bibliography

- [1] D. Varghese, Y. Xuan, Y. Q. Wu, T. Shen, P. D. Ye, and M. A. Alam, in *Proceedings of International Electron Devices Meeting Technical Digest*, 379–382 (2008).
- [2] G. Brammertz, H.-C. Lin, M. Caymax, M. Meuris, M. Heyns, and M. Passlack, *Appl. Phys. Lett.* **95**, 202109 (2009).
- [3] R. Engel-Herbert, Y. Hwang, and S. Stemmer, *J. Appl. Phys.* **108**, 124101 (2010).
- [4] L. K. Chu, C. Merckling, A. Alian, J. Dekoster, J. Kwo, M. Hong, M. Caymax, and M. Heyns, *Appl. Phys. Lett.* **99**, 042908 (2011).
- [5] V. Djara, T. P. O'Regan, K. Cherkaoui, M. Schmidt, S. Monaghan, É. O'Connor, I. M. Povey, D. O'Connell, M. E. Pemble, and P. K. Hurley, *Microelectronic Engineering* **109**, 182 (2013).
- [6] D. R. Lide, *CRC Handbook of Chemistry and Physics* (CRC, Boca Raton, 2007).
- [7] G. Brammertz, H. C. Lin, K. Martens, D. Mercier, C. Merckling, J. Penaud, C. Adelman, S. Sioncke, W. E. Wang, M. Caymax, M. Meuris, and M. Heyns, *Journal of The Electrochemical Society*, **155**(12), H945-H950 (2008).
- [8] L. A. Walsh, G. Hughes, P. K. Hurley, J. Lin, and J. C. Woicik, *Appl. Phys. Lett.* **101**, 241602 (2012).
- [9] L. A. Walsh, G. Hughes, J. Lin, P. K. Hurley, T. P. O'Regan, E. Cockayne, and J. C. Woicik, *Phys. Rev. B* **88**(4), 045322 (2013).
- [10] E. O'Connor, B. Brennan, V. Djara, K. Cherkaoui, S. Monaghan, S. B. Newcomb, R. Contreras, M. Milojevic, G. Hughes, M. E. Pemble, R. M. Wallace, and P. K. Hurley, *J. Appl. Phys.* **109**, 024101 (2011).
- [11] Y. Y. Gomeniuk, A. N. Nazarov, S. Monaghan, K. Cherkaoui, E. O'Connor, I. Povey, V. Djara, and P. K. Hurley, *Proceedings of the International Conference on Nanomaterials: Applications and Properties* (2012), vol. **1**, no. 3, p. 03TF16.
- [12] K. Kakushima, K. Okamoto, K. Tachi, J. Song, S. Sato, T. Kawanago, K. Tsutsui, N. Sugii, P. Ahmet, T. Hattori, and H. Iwai, *J. Appl. Phys.* **104**, 104908 (2008).

- [13] K. Kobayashi, Nucl. Instrum. Methods Phys. Res., Sect. A **601**(1–2), 32–47 (2009).
- [14] S. Tanuma, C. J. Powell, and D. R. Penn, Surf. Interface Anal. **43**(3), 689–713 (2011).
- [15] J. Chastain and J. F. Moulder, Handbook of X-ray Photoelectron Spectroscopy: A Reference Book of Standard Spectra for Identification and Interpretation of XPS Data (Physical Electronics, Eden Prairie, Minnesota, 1995).
- [16] E. H. Nicollian and J. R. Brews, MOS Physics and Technology (Wiley, New York, 2003).
- [17] S. M. Sze and K. K. Ng, Physics of Semiconductor Devices (Wiley, NJ, 2007).
- [18] P. K. Hurley, E. O'Connor, S. Monaghan, R. D. Long, A. O'Mahony, I. M. Povey, K. Cherkaoui, J. MacHale, A. J. Quinn, and G. Brammertz, M. Heyns, S. B. Newcomb, V. V. Afanas'ev, A. M. Sonnet, R. V. Galatage, M. N. Jivani, E. M. Vogel, R. M. Wallace and M. E. Pemble, ECS Trans. **25**(6), 113 (2009).
- [19] A. O'Mahony, S. Monaghan, G. Provenzano, I. M. Povey, M. G. Nolan, E. O'Connor, K. Cherkaoui, S. B. Newcomb, F. Crupi, P. K. Hurley, and M. E. Pemble, Appl. Phys. Lett. **97**, 052904 (2010).
- [20] S. Klejna and S. D. Elliott, J. Phys. Chem. C **116**(1), 643–654 (2012).
- [21] A. Bahari, P. Morgen, and Z. S. Li, Surf. Sci. **600**(15), 2966–2971 (2006).
- [22] M. Gaowei, E. M. Muller, A. K. Rumaiz, C. Weiland, E. Cockayne, J. Jordan-Sweet, J. Smedley, and J. C. Woicik, Appl. Phys. Lett. **100**, 201606 (2012).
- [23] R. D. Long, B. Shin, S. Monaghan, K. Cherkaoui, J. Cagnon, S. Stemmer, P. C. McIntyre, and P. K. Hurley, J. Electrochem. Soc. **158**, G103 (2011).
- [24] G. Brammertz, H. C. Lin, K. Martens, A. Alian, C. Merckling, J. Penaud, D. Kohen, W.-E. Wang, S. Sioncke, A. Delabie, M. Meuris, M. Caymax, and M. Heyns, Electrochem. Soc. Trans. **19**(5), 375–386 (2009).
- [25] N. Taoka, M. Yokoyama, S. H. Kim, R. Suzuki, R. Iida, S. Lee, T. Hoshii, W. Jevasuwan, T. Maeda, T. Yasuda, O. Ichikawa, N. Fukuhara, M.

Hata, M. Takenaka, and S. Takagi, in Proceedings of the IEEE International Electron Devices Meeting (IEDM) (IEEE, 2011), p. 610.

[26] H. C. Lin, W. E. Wang, G. Brammertz, M. Meuris, and M. Heyns, *Microelectronic Engineering* **86**(7–9), 1554–1557 (2009).

[27] C. A. Lin, H. C. Chiu, T. H. Chiang, T. D. Lin, Y. H. Chang, W. H. Chang, Y. C. Chang, W. E. Wang, J. Dekoster, T. Y. Hoffmann, M. Hong, and J. Kwo, *Appl. Phys. Lett.* **98**, 062108 (2011).

[28] W. Melitz, J. Shen, S. Lee, J. S. Lee, A. C. Kummel, R. Droopad, and E. T. Yu, *J. Appl. Phys.* **108**, 023711 (2010).

Chapter 7: Conclusions and Future Outlook

7.1 Conclusions of Work Presented in Thesis

The primary aim of this thesis was to examine electrically active defects in the metal/high- k /In_{0.53}Ga_{0.47}As MOS systems. The study was focused on the characteristics of border traps which are located in the interfacial transition layer between the high- k oxide the crystalline In_{0.53}Ga_{0.47}As and now represent one of the main challenges for the development of the high- k /In_{0.53}Ga_{0.47}As gate stacks, and furthermore, to investigate possible passivation methods to resolve the reliability issues caused by border traps. The study of border traps (or charge trapping) was carried out using C-V hysteresis measurements in either HfO₂/In_{0.53}Ga_{0.47}As or Al₂O₃/In_{0.53}Ga_{0.47}As MOS capacitors with various metal gate electrodes, where the high- k oxides were deposited using ALD.

The charge trapping behavior is observed to be predominantly a reversible process (or a temporary trapping process) and the density of trapped charge estimated from C-V hysteresis window can be comparable to, or even greater than the typical high- k /In_{0.53}Ga_{0.47}As interface state density, highlighting the importance of C-V hysteresis in the high- k /In_{0.53}Ga_{0.47}As MOS system. It is also observed that the p -type In_{0.53}Ga_{0.47}As MOS samples exhibit a larger C-V hysteresis and permanent charge trapping than their n -type In_{0.53}Ga_{0.47}As counterparts, possibly resulting from a higher density of border traps with energy levels aligned with the valence band edge than that with the conduction band edge and/or a higher barrier height for the trapped holes to be removed from the trapping sites than the case of trapped electrons.

Based on TEM analysis, it is observed that the use of an Al gate in $\text{HfO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ samples results in the formation of an Al_2O_3 layer at the top Al/ HfO_2 interface which has a “scavenging” effect on the interfacial transition layer between the HfO_2 and the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ surface. This results in a significant reduction in C-V hysteresis and charge trapping when compared to a Pt gate $\text{HfO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ sample, in which $\sim 1\text{nm}$ of interface oxide is observed in areas with and without metallization. In addition, $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS systems, which have no detectable interface oxide due to the reported “self-cleaning” effect of Al_2O_3 by ALD, exhibit a relatively low level of C-V hysteresis compared to $\text{HfO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS systems. These experimental observations indicate that the charge trapping is predominately taking place near/at the interfacial transition region between the high- k oxide and the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ substrate, which can contain native oxides of In, Ga and As.

Based on an oxide thickness series, it is demonstrated that the C-V hysteresis increases linearly with the increasing high- k oxide thickness for both $\text{HfO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS systems, with the corresponding trapped charge density (Q_{trapped}) being a constant value over all the oxide thicknesses. This result indicates that the trapped charge is predominately localized as a sheet/line charge (in cm^{-2}) near/at the high- $k/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface and is not distributed throughout the high- k oxide (in cm^{-3}). All the experimental results presented in this work identify the origin of C-V hysteresis and charge trapping is in the interfacial transition layer between the high- k oxide and the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, and thus the engineering of this very interface is the key to reducing C-V hysteresis and reduce device instability in the high- $k/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ based MOS devices.

The kinetics of charge trapping was explored through C-V hysteresis with a varying stress time (or hold time) at V_{max} in accumulation. It is observed in $\text{Al}/\text{Al}_2\text{O}_3(8\text{nm})/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS structures that the C-V hysteresis increases with a power law dependence with the stress time (up to 2000s) and the charge trapping efficiency decreases with a power law dependence with the increasing injected charge density. Similar measurements were performed

for Pd/HfO₂(15nm)/In_{0.53}Ga_{0.47}As MOS structure with a much longer stress time applied. Due to a large C-V hysteresis with $t_{\text{stress}}=0$ (i.e. ΔV_0) for HfO₂/In_{0.53}Ga_{0.47}As, $\Delta V - \Delta V_0$ is plotted as a function of t_{stress} . It is observed that $\Delta V - \Delta V_0$ increases with a power law dependence on stress time at V_{max} at the initial stage of stressing and approaches to a plateau at sufficiently long stress times, implying that the filling of almost all the trapping states energy levels is achieved, and additional new border traps were not being created using the stressing time and electric fields explored in the thesis. In addition, a larger V_{max} used in C-V hysteresis results in a higher level of charge trapping due to additional border traps being accessed at a higher oxide field induced by the larger V_{max} , and because the Fermi level is at a higher energy above the In_{0.53}Ga_{0.47}As conduction band edge. Moreover, measurements were performed to analyze charge trapping relaxation. It is demonstrated that a significant portion of trapped charge is removed from the trapping sites within ~4s after the stress gate voltage is removed in high- k /In_{0.53}Ga_{0.47}As MOS systems. The relaxation process for high- k /In_{0.53}Ga_{0.47}As is found to be much faster than that for high- k /Si MOS devices.

In this thesis, a systematic study of the effect of forming gas annealing (5% H₂ / 95% N₂) at a series of temperatures (250⁰C, 300⁰C, 350⁰C, 400⁰C and 450⁰C) for 30min on the electrical characteristics was performed on Au/Ni gate contacts over both HfO₂(8nm)/In_{0.53}Ga_{0.47}As and Al₂O₃(8nm)/In_{0.53}Ga_{0.47}As MOS capacitors. It is observed that for HfO₂/ n -In_{0.53}Ga_{0.47}As MOS system that FGA at all temperatures under investigation improved the multi-frequency C-V responses in terms of accumulation frequency dispersion, C-V stretch-out and D_{it} responses in the nominal inversion region. The accumulation frequency dispersion goes through a minimum with increasing FGA temperature for the HfO₂/ n -In_{0.53}Ga_{0.47}As MOS system. For HfO₂/ p -In_{0.53}Ga_{0.47}As MOS structures, multi-frequency C-V responses are only improved for FGA 250⁰C to 350⁰C and increasing FGA temperature ($\geq 400^0\text{C}$) increases the accumulation frequency dispersion. For Al₂O₃/ n -In_{0.53}Ga_{0.47}As MOS capacitors, accumulation frequency dispersion decreases with increasing FGA temperature and C-V stretch-out is also

improved following the FGA. The most enhanced C-V characteristics are observed for the sample treated with FGA 450⁰C, where the estimated D_{it} is $\sim 2.19 \times 10^{11} \text{cm}^{-2} \text{eV}^{-1}$ near the conduction band edge, which is about an order of magnitude lower than the $\text{Al}_2\text{O}_3/n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ sample with no FGA. For the case of $\text{Al}_2\text{O}_3/p\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS system, there is no significant improvement in multi-frequency C-V responses following the FGA.

C-V hysteresis (or Q_{trapped}) was also investigated as a function of overdrive voltage (V_{ov}) for samples treated with the FGA temperature series. It is shown that the voltage acceleration factor (γ -factor) for $\text{HfO}_2/n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ treated with FGA 300⁰C and 350⁰C are slightly improved when compared with other FGA conditions, indicating that the energy spread of the border traps is narrowed resulting in reduced Q_{trapped} at low V_{ov} . For the $\text{HfO}_2/p\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS system, the no FGA sample cannot reach the flatband capacitance within the gate bias range which can be used prior to excessive gate leakage currents, therefore it is impossible to compare Q_{trapped} under the same oxide field. For Al_2O_3 samples, the γ -factor changes slightly over different FGA conditions for both $n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ and $p\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ therefore it is assumed that the γ -factor remains constant, suggesting that FGA does not change the energy distribution of border traps. It is shown that FGA at all temperatures reduce Q_{trapped} for $\text{Al}_2\text{O}_3/n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$. In the case of the $\text{Al}_2\text{O}_3/p\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$, FGA at 250⁰C and 300⁰C have negligible effect on Q_{trapped} , however, $\text{FGA} \geq 350^0\text{C}$ increases Q_{trapped} .

The effect of both FGA (at 400⁰C for 5min) and the optimized 10% $(\text{NH}_4)_2\text{S}$ surface passivation on C-V hysteresis for $\text{TiN}/\text{Al}_2\text{O}_3(4\text{nm})/n\text{-In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitor was also studied. It has been shown that while the 10% $(\text{NH}_4)_2\text{S}$ surface passivation has a very limited effect on the C-V hysteresis, the FGA (400⁰C, 5min) reduces the C-V hysteresis significantly. Treatment with both FGA (400⁰C, 5min) and the 10% $(\text{NH}_4)_2\text{S}$ surface passivation results in the most reduced C-V hysteresis and associated charge trapped.

Combined C-V and HAXPES analysis have been made on $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors with both Ni and Al metal gates, which have high and low work functions, respectively. It is observed from HAXPES that there is a band bending prior to metal deposition due to a combination of fixed oxide charges and possible donor-type interface states. The substrate core level binding energy (BE) shifts in the expected directions following the deposition of both high and low work function metals. Fermi level positions at zero gate bias are calculated using both C-V and HAXPES analysis and a reasonable agreement has been achieved between the two techniques. This work links the electronic and chemical properties at a buried oxide/semiconductor interface in an MOS system, and is useful as it allows an independent method to calculate the surface Fermi level position in a III-V MOS structure, which is needed to map the gate voltage to the surface Fermi level position for D_{it} extraction across the energy gap. There is also a shift in BE of the oxide core levels following metal deposition, which is caused by the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ surface Fermi level movement and a change in the potential drop across the Al_2O_3 , and the shifts are in the expected directions. The broadening of the oxide peak widths indicates a higher potential drop across the Al_2O_3 layer with Ni gate than that with Al gate.

7.2 Future Outlook

In chapter 4, C-V hysteresis as a function of stress time (up to 100,000s) has been investigated for $\text{HfO}_2(15\text{nm})/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS systems. It is worth performing C-V hysteresis measurement for $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS systems with sufficiently long stress time in accumulation and investigate the relation between C-V hysteresis and stress time and see if the power law dependence can be observed at the initial stage of stressing and a plateau region can be reached at sufficiently long stress times. Moreover, due to the high density of defect states in HfO_2 film and at/near the $\text{HfO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface, the current during stress exhibits high levels of noise and instability, and it is impossible to obtain the injected charge density using the measured gate current during the stress time at V_{max} (i.e. the maximum gate voltage in accumulation in C-V hysteresis). The $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$

structures exhibit more stable current-time characteristics during stress, and therefore measuring gate current versus time (up to 100ks) and calculating Q_{injected} is possible. Combining the C-V hysteresis measurements with sufficiently long stress times in accumulation for $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS systems, it should be possible to build a Q_{trapped} versus Q_{injected} model, where information such as trap cross section can be extracted.

The FGA work presented in this thesis can be extended for further analysis into high- $k/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS systems and finally to find the optimized surface treatment approach to minimize the density of interface states and C-V hysteresis. Some suggested future work is listed below.

1) D_{it} calculation using full conductance method for FGA temperature series

In this work, D_{it} was calculated using high-low frequency capacitance method for the FGA temperature series (at 250°C ~ 450°C for 30min) for both $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and $\text{HfO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS systems. A full conductance method as mentioned in chapter 2 can be used in the future work to extract more accurate D_{it} values and the corresponding energy levels. Sweeping frequency at a series of V_g values in depletion in the full conductance method should be used as the C-V sweeps at multiple frequencies can result in charge trapping associated C-V shift and also stress induced interface states especially in the case of high defect states MOS systems such as $\text{HfO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS structures.

The analysis could also be extended to extract both the interface state density and border trap density and profile into the conduction band from the multi-frequency C-V results using the Sentaurus software [1]. This software package can input an interface state density throughout the energy gap, and into the conduction band, and can also vary the electron and hole capture cross sections. In addition, the software can incorporate recently developed models to take into account the capacitance and conductance of associated with border traps in the oxide which communicate with electrons and holes in the conduction and valance bands.

2) Extending the analysis to bi-layer and tri-layer oxide systems on $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$

The work in this thesis examined C-V hysteresis in either $\text{HfO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ or $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors. It could be extended to examine bi-layer gate oxide systems such as $\text{HfO}_2/\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, which have been demonstrated to achieve reduced interface state density values combined with scaled equivalent oxide thickness [2]. Another possibility is that while all experimental evidence points to charge trapping occurring near the oxide/ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface, it is possible that the initial charge injection occurs at the metal/oxide interface, with the trapping near the oxide/oxide/ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface. This could be of particular relevance for the case of a $\text{HfO}_2/\text{Al}_2\text{O}_3$ gate stack, where the barrier to charge injection is lower at the metal/oxide contact.

3) Extension on FGA temperature using millisecond annealing.

The maximum temperature used in the FGA temperature series in this work was 450°C . Going to higher values is problematic, as the annealing at 450°C results in a significant increase in gate leakage. This increase is most probably due to diffusion of the substrate elements (particularly Indium) into the gate oxide at temperatures above 400°C [3, 4]. One possible route to optimize the post deposition annealing, is to move to very rapid thermal anneals in the millisecond regime, which can be achieved by flash annealing. This allows the temperature to be increased, while minimizing the overall thermal budget which governs diffusion.

4) C-V hysteresis and interface states analysis for FGA time series

Based on the FGA temperature series (30min), selected FGA temperature can be extended to a time series (10min, 20min and 30min) sample set, on which interface states and C-V hysteresis analysis will be performed. The combination of FGA temperature series and time series will be useful to investigate the optimum FGA condition (time and temperature) to minimize interface states and border traps.

Finally, the thesis demonstrated how HAXPES can be combined with C-V analysis of MOS structures to investigate and quantify the Fermi level position at buried interfaces in MOS structures. This analysis was performed for HAXPES with no bias, where metals with differing work function values were used to modulate the surface Fermi level at zero bias. In principle, the technique could be extended to biased HAXPES, allowing C-V and HAXPES to be compared over a range of surface potentials. This could be of interest to various high- k /III-V MOS systems (e.g., InGaAs, InAs and GaSb) as well as emerging studies on MOS systems formed on 2D semiconductors.

Bibliography

- [1] http://nadin.miem.edu.ru/Sentaurus_Training_2014/index.html
- [2] A. O'Mahony, S. Monaghan, G. Provenzano, I. M. Povey, M. G. Nolan, É. O'Connor, K. Cherkaoui, S. B. Newcomb, F. Crupi, P. K. Hurley, and M. E. Pemble, Appl. Phys. Lett. **97**, 052904 (2010).
- [3] W. Cabrera, B. Brennan, H. Dong, T. P. O'Regan, I. M. Povey, S. Monaghan, E. O'Connor, P. K. Hurley, R. M. Wallace, Y. J. Chabal, Appl. Phys. Lett. **104**, 011601 (2014).
- [4] Igor Krylov, Arkady Gavrilov, Moshe Eizenberg, and Dan Ritter, Appl. Phys. Lett. **103**, 053502 (2013).

Appendix I: Publications and Conference

Presentations

Publications (directly related to PhD thesis)

1. ‘An investigation of capacitance-voltage hysteresis in metal/high- k /In_{0.53}Ga_{0.47}As metal-oxide-semiconductor capacitors’, **Jun Lin**, Yuri Y. Gomeniuk, Scott Monaghan, Ian M. Povey, Karim Cherkaoui, Éamon O'Connor, Máire Power, and Paul K. Hurley, *Journal of Applied Physics*, **114**,144105 (2013).
2. ‘A study of capacitance-voltage hysteresis in the HfO₂/InGaAs metal-oxide-semiconductor system’, **Jun Lin**, Scott Monaghan, Karim Cherkaoui, Ian Povey, Éamon O'Connor, Brendan Sheehan, and Paul Hurley, *Microelectronic Engineering*, **147** (2015) 273–276.
3. ‘A study of capacitance-voltage hysteresis in HfO₂/InGaAs metal-oxide-semiconductor systems’, **Jun Lin**, Scott Monaghan, Karim Cherkaoui, Ian M. Povey, Éamon O'Connor, Brendan Sheehan and Paul K. Hurley, *Proceedings of IIRW*, 36 (2014).
4. ‘A combined capacitance-voltage and hard x-ray photoelectron spectroscopy characterisation of metal/Al₂O₃/In_{0.53}Ga_{0.47}As capacitor structures’, **Jun Lin**, Lee Walsh, Greg Hughes, Joseph C. Woicik, Ian M. Povey, Terrance P. O'Regan, and Paul K. Hurley, *Journal of Applied Physics*, **116**, 024104 (2014).
5. ‘Hard x-ray photoelectron spectroscopy and electrical characterization study of the surface potential in metal/Al₂O₃/GaAs(100) metal-oxide-semiconductor structures’, Lee Walsh, Greg Hughes, **Jun Lin**, Paul K. Hurley, Terrance P. O'Regan, Eric Cockayne and Joseph C. Woicik, *Physical Review B* **88**(4), 045322 (2013).
6. ‘A combined hard x-ray photoelectron spectroscopy and electrical characterisation study of metal/SiO₂/Si(100) metal-oxide-semiconductor structures’, Lee A. Walsh, Greg Hughes, Paul K. Hurley, **Jun Lin**, and Joseph C. Woicik, *Applied Physics Letter*, **101**, 241602 (2012).

7. 'The Characterization and Passivation of Fixed Oxide Charges and Interface States in the $\text{Al}_2\text{O}_3/\text{InGaAs}$ MOS System', Paul K. Hurley, Éamon O'Connor, Vladimir Djara, Scott Monaghan, Ian M. Povey, Rathnait D. Long, Brendan Sheehan, **Jun Lin**, Paul C. McIntyre, Barry Brennan, Robert M. Wallace, Martyn E. Pemble and Karim Cherkaoui, IEEE Transactions on Device and Materials Reliability, vol. **13**, no. 4, December 2013.
8. 'Electrical and physical characterization of the $\text{Al}_2\text{O}_3/\text{p-GaSb}$ interface for 1%, 5%, 10%, and 22% $(\text{NH}_4)_2\text{S}$ surface treatments', Uthayasankaran Peralagu, Ian M. Povey, Patrick Carolan, **Jun Lin**, Rocio Contreras-Guerrero, Ravi Droopad, Paul K. Hurley, and Iain G. Thayne, Applied Physics Letters, **105**, 162907 (2014).
9. 'Can Metal/ $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ MOSCAP Properties Translate to Metal/ $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ MOSFET Characteristics?', Karim Cherkaoui, Vladimir Djara, Éamon O'Connor, **Jun Lin**, Muhammad A. Negara, Ian M. Povey, Scott Monaghan, and Paul K. Hurley, ECS Transactions, **45**(3) 79-88 (2012).

Oral presentations at International Conferences

1. Oral presentation at WoDiM 2012, Dresden, Germany: 'An investigation of charge trapping in metal/high- $k/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ metal-oxide-semiconductor capacitors', **Jun Lin**, Yuri Y. Gomeniuk, Scott Monaghan, Karim Cherkaoui, Eamon O'Connor, Ian Povey and Paul K. Hurley
2. Oral presentation at MRS 2014, San Francisco, USA: 'A combined study of the metal/ $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS system using capacitance-voltage characterization and hard x-ray photoelectron spectroscopy', **Jun Lin**, Lee Walsh, Greg Hughes, Joseph C. Woicik, Ian M. Povey and Paul K. Hurley
3. Oral presentation at WoDiM 2014, Kinsale, Ireland: 'An investigation of charge trapping in metal/high- k/InGaAs MOS system using capacitance-voltage hysteresis', **Jun Lin**, Yuri Y. Gomeniuk, Scott Monaghan, Ian M. Povey, Karim Cherkaoui, Éamon O'Connor, Brendan Sheehan and Paul K. Hurley

4. Oral presentation at IIRW 2014, South Lake Tahoe, USA: ‘An investigation of charge trapping in metal/high- k /InGaAs MOS system using capacitance-voltage hysteresis’, **Jun Lin**, Yuri Y. Gomeniuk, Scott Monaghan, Ian M. Povey, Karim Cherkaoui, Éamon O’Connor, Brendan Sheehan and Paul K. Hurley
5. Oral presentation at INFOS 2015, Udine, Italy: ‘A study of capacitance-voltage hysteresis in the high- k /InGaAs metal-oxide-semiconductor system’, **Jun Lin**, Yuri Y. Gomeniuk, Scott Monaghan, Ian Povey, Karim Cherkaoui, Éamon O’Connor, Brendan Sheehan, and Paul Hurley

Poster presentations

1. Poster presentation at Intel European Research and Innovation Conference (ERIC) 2011, Intel, Leixlip, Ireland: ‘An investigation of capacitance-voltage hysteresis in the high- k /In _{x} Ga _{$1-x$} As MOS system’, **Jun Lin**, Yuri Y. Gomeniuk, Scott Monaghan, Karim Cherkaoui, Eamon O’Connor, Ian Povey and Paul K. Hurley
2. Poster presentation at Intel Ireland Research Conference (IIRC) 2012, Croke Park, Dublin, Ireland: ‘An investigation of charge trapping in high- k /InGaAs MOS system’, **Jun Lin**, Yuri Y. Gomeniuk, Scott Monaghan, Karim Cherkaoui, Eamon O’Connor, Ian M. Povey and Paul K. Hurley
3. Poster presentation at Intel Ireland Research Conference (IIRC) 2013, Clontarf Castle, Dublin, Ireland: ‘A combined study of the metal/Al₂O₃/InGaAs MOS system using capacitance-voltage characterization and hard x-ray photoelectron spectroscopy’, **Jun Lin**, Lee A. Walsh, Greg Hughes, Joseph C. Woicik, and Paul K. Hurley
4. Poster presentation in Tyndall Poster Competition 2015, Tyndall National Institute, Ireland: ‘A study of border traps in high- k /In_{0.53}Ga_{0.47}As MOS systems using capacitance-voltage hysteresis’, **Jun Lin**, Scott Monaghan, Karim Cherkaoui, Ian Povey, Éamon O’Connor, Brendan Sheehan, and Paul Hurley

5. Poster presentation at WoDiM 2016, Catania, Italy: ‘The effect of forming gas annealing on C-V hysteresis in the high- k /In_{0.53}Ga_{0.47}As MOS system’, **Jun Lin**, Scott Monaghan, Karim Cherkaoui, Ian Povey, Brendan Sheehan, Jacopo Franco, and Paul Hurley

Appendix II: Calculations of Sample Properties

k_B = Boltzmann's Constant = $8.617 \times 10^{-5} \text{ eV/K} = 1.38 \times 10^{-23} \text{ JK}^{-1}$

T = temperature in Kelvin

q = elementary charge = $1.6 \times 10^{-19} \text{ C}$

n_i = intrinsic carrier concentration = $6.3 \times 10^{11} \text{ cm}^{-3}$ at room temperature for $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$

N_{doping} = doping level of semiconductor = $4 \times 10^{17} \text{ cm}^{-3}$ for $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ used in this work

N_v = valance band density of states = $7.7 \times 10^{18} \text{ cm}^{-3}$ for $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$

N_c = conduction band density of states = $2.1 \times 10^{17} \text{ cm}^{-3}$ for $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$

E_g = bandgap energy = 0.75 eV for $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$

ϵ_0 = vacuum permittivity = $8.854 \times 10^{-14} \text{ F/cm}$

ϵ_s = relative permittivity of semiconductor = 13.77 for $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$

(1) Bulk Fermi level position and Fermi level position at the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ surface at flatband condition

Bulk potential: $|\Phi_B| = \frac{k_B T}{q} \ln\left(\frac{N_{\text{doping}}}{n_i}\right)$

Fermi level position for n -type: $E_f - E_v = (E_i - E_v) + |\Phi_B|$

Fermi level position for p -type: $E_f - E_v = (E_i - E_v) - |\Phi_B|$

Intrinsic Fermi level position: $E_i - E_v = \frac{E_g}{2} + \frac{k_B T}{2} \ln\left(\frac{N_v}{N_c}\right) \approx \frac{E_g}{2}$

(2) Fermi level position at $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ surface calculated from measured capacitance in depletion

Semiconductor differential capacitance:

$$\frac{1}{C_s} = \frac{1}{C_m} - \frac{1}{C_{ox}} \text{ or } C_s = \frac{C_{ox} \times C_m}{C_{ox} - C_m}$$

Depletion layer width: $w = \frac{\epsilon_s \epsilon_0}{C_s}$

Absolute value of surface potential: $|\Psi_s| = \frac{q N_{\text{doping}} w^2}{2 \epsilon_s \epsilon_0}$

For n -type in depletion, $E_f - E_v = (E_i - E_v) + |\Phi_B| - |\Psi_s|$

For p -type in depletion, $E_f - E_v = (E_i - E_v) - |\Phi_B| + |\Psi_s|$

(3) Minimum capacitance

The minimum capacitance (C_{\min}) occurs in depletion when the depletion layer width reaches its maximum, i.e. MOS capacitor reaches the onset of strong inversion.

Surface potential at the onset of strong inversion:

$$|\Psi_s| = 2|\Phi_B| = \frac{2k_B T}{q} \ln\left(\frac{N_{\text{doping}}}{n_i}\right)$$

Surface potential at the onset of strong inversion can also be expressed using the maximum depletion layer width (w_{\max})

$$|\Psi_s| = \frac{qN_{\text{doping}}w_{\max}^2}{2\epsilon_0\epsilon_s}$$

The above two equations yield the maximum depletion layer width

$$w_{\max} = \sqrt{\frac{4\epsilon_0\epsilon_s k_B T}{q^2 N_{\text{doping}}} \ln\left(\frac{N_{\text{doping}}}{n_i}\right)}$$

Minimum capacitance of the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ substrate:

$$C_{\min_InGaAs} = \frac{\epsilon_0\epsilon_s}{w_{\max}}$$

Minimum capacitance of the high- $k/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitor:

$$C_{\min} = \frac{C_{\text{ox}} \times C_{\min_InGaAs}}{C_{\text{ox}} + C_{\min_InGaAs}}$$

(4) Flatband capacitance and flatband voltage

4a) C_{fb}

Debye length:

$$\lambda_D = \sqrt{\frac{\epsilon_0\epsilon_s k_B T}{q^2 N_{\text{doping}}}}$$

Flatband capacitance of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$:

$$C_{\text{InGaAs_fb}} = \frac{\epsilon_0 \epsilon_s}{\lambda_D}$$

Flatband capacitance of high- $k/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitor:

$$C_{\text{fb}} = \frac{C_{\text{ox}} \times C_{\text{InGaAs_fb}}}{C_{\text{ox}} + C_{\text{InGaAs_fb}}}$$

4b) V_{fb}

Flatband voltage (V_{fb}) can be read off from the true high frequency C-V characteristic where the interface states associated capacitance (C_{it}) is negligible. To obtain a true high frequency, measurements should be carried out at the lowest temperature and highest frequency where possible.

Appendix III: Electron Paramagnetic Resonance

Electron Paramagnetic Resonance (EPR) is a technique for studying chemical species with one or more unpaired electrons. As part of the PhD, EPR measurements and analysis were performed under the supervision of Dr. Robert Barklie in Trinity College Dublin, aiming to get trainings to carry out EPR measurement, and to use EPR to study high- k /Si interface. Furthermore, EPR was performed on high- k /In_{0.53}Ga_{0.47}As systems.

Figure III-1 (a) and (b) shows the EPR signal detected from an uncapped HfO₂/Si(111) sample which are as-deposited and treated by rapid thermal annealing (RTA), respectively.

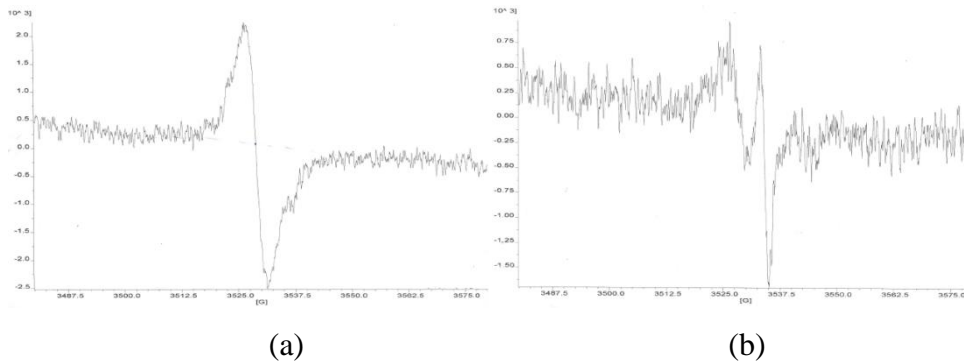


Figure III-1: EPR of HfO₂/Si(111) (a) without any annealing approach and (b) with RTA.

The signal around the centre field in Figure III-1(a) is the EPR signal of the Si dangling bonds at the damaged sample edges which has a calculated spin population of about 2.55×10^{13} . For the sample after RTA treatment shown in Figure III-1(b), two signals were observed. The field at which the signal on the left occurred is the same as that of the sample without RTA. Therefore this signal is also from Si dangling bonds located at the edge of the sample piece with an estimation of spin population of about 3.73×10^{12} . As compared with the number of spins in the HfO₂/Si(111) sample without RTA, the amount of Si dangling bonds is reduced by almost an order of magnitude after RTA. The EPR signal detected at the higher field (i.e. the signal on the right hand side in Figure III-1(b)) is from the P_b centre originating from

HfO₂/Si(111) interface that has a spin population of 4.5×10^{11} . As the RTA significantly reduces the number of Si dangling bonds at the damaged sample edge, the EPR signal of the P_b centre becomes visible.

EPR measurements were also carried out on high-*k*/In_{0.53}Ga_{0.47}As/semi-insulating InP(100) structure (see Figure III-2). Either HfO₂ or Al₂O₃ of 10nm is deposited by ALD as the high-*k* oxide on the *n*-, *p*- or undoped In_{0.53}Ga_{0.47}As(0.5μm).

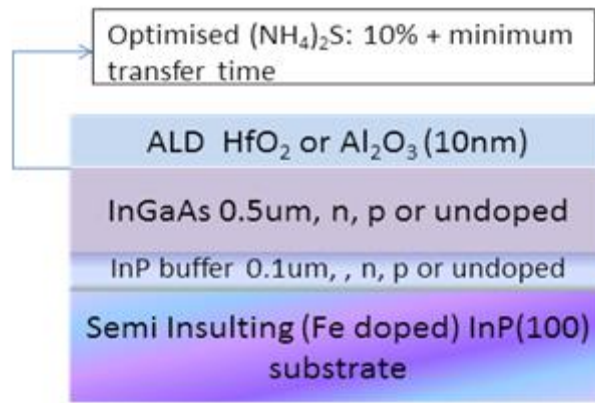


Figure III-2: High-*k*/In_{0.53}Ga_{0.47}As sample structure for EPR measurements.

All the samples exhibited similar EPR signals. An example is shown in Figure III-3. The signal around 3500G is the EPR signal from the cavity where the sample is placed, possibly due to contamination in the cavity as a similar signal is detected with no sample in the cavity. The two peaks on both sides of the centre signal are the EPR signals which are possibly originates from Fe³⁺ in the semi-insulating InP(100) substrate. Moreover, these two peaks are observed to be dependent on the direction of the external magnetic field, giving further proof of Fe³⁺ in the InP being the origin of the detected EPR signals. No EPR signals from the interface defects between the high-*k* oxide and In_{0.53}Ga_{0.47}As are detected. The EPR signal of the interface defects could be lost in the Fe³⁺ signal which has a large intensity. In addition, all the stable isotopes of In, Ga and As have a nuclear spin, which will broaden the EPR signal and reduce the signal height for a given signal intensity, the EPR

signal from the high- k /In_{0.53}Ga_{0.47}As interface defects is likely to be lost in the noise.

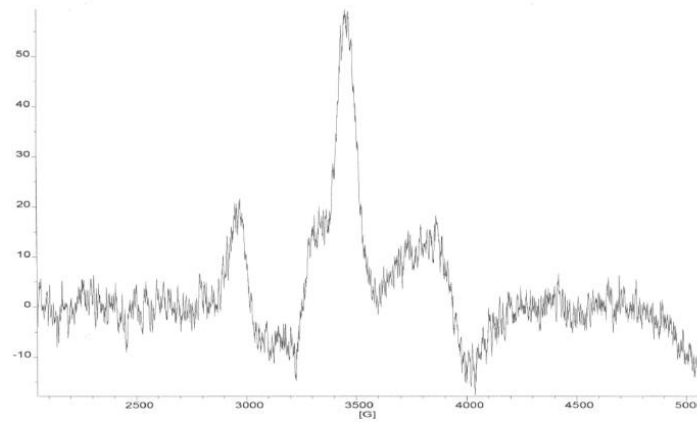


Figure III-3: EPR of Al₂O₃/n-In_{0.53}Ga_{0.47}As/InP structure.

In order to further verify that the two signals on both sides of the centre signal come from the InP(100) substrate, the samples were attached to the spin free quartz plates using spin free wax and were then placed in HCl to etch away the semi-insulating InP. The EPR measurements on the samples with InP removed have demonstrated that the two side signals are removed, as expected. However, the high- k /In_{0.53}Ga_{0.47}As interface signal is still not observed.

Appendix IV: Power Law Dependence of η_{trapping} on Q_{injected}

The threshold voltage shift versus injected charge density model for MOSFET established by Zafar *et al* is expressed below.

$$\Delta V_T = \Delta V_{\text{max}} \times [1 - \exp(-(Q_{\text{injected}}\sigma_0)^\beta)]$$

where ΔV_T is the threshold voltage shift, Q_{injected} is the density of injected charge, σ_0 is the characteristic capture cross section for the ensemble of traps with a continuous distribution in cross section, and β is a measure of the distribution width.

For MOS capacitor structure, if Zafar's model still holds, ΔV_T can be replaced by ΔV

$$\Delta V = \Delta V_{\text{max}} \times [1 - \exp(-(Q_{\text{injected}}\sigma_0)^\beta)]$$

where ΔV is the C-V hysteresis measured on MOS capacitor.

At the initial stage of stressing where $Q_{\text{injected}} \ll 1/\sigma_0$,

$$\Delta V = \Delta V_{\text{max}} \times (Q_{\text{injected}}\sigma_0)^\beta$$

which can be rewritten as $\Delta V = (\Delta V_{\text{max}} \times \sigma_0^\beta) \times Q_{\text{injected}}^\beta$, and this indicates that ΔV increases with a power law dependence on Q_{injected} for short stress times.

Charge trapping efficiency is defined as

$$\eta_{\text{trapping}} = \frac{Q_{\text{trapped}}}{Q_{\text{injected}}} \times 100\%$$

Therefore, $Q_{\text{trapped}} = \eta_{\text{trapping}} Q_{\text{injected}}$. In addition, $Q_{\text{trapped}} = \Delta V \times C_{\text{ox}}/q$, equating $\eta_{\text{trapping}} Q_{\text{injected}}$ and $(\Delta V \times \frac{C_{\text{ox}}}{q})$ yields

$$\Delta V = \frac{q\eta_{\text{trapping}} Q_{\text{injected}}}{C_{\text{ox}}}$$

Combing the above equation with $\Delta V = (\Delta V_{\text{max}} \times \sigma_0^\beta) \times Q_{\text{injected}}^\beta$ at the initial stage of stressing,

$$\frac{q\eta_{\text{trapping}}Q_{\text{injected}}}{C_{\text{ox}}} = (\Delta V_{\text{max}} \times \sigma_0^\beta) \times Q_{\text{injected}}^\beta$$

Rearranging the above equation yields

$$\eta_{\text{trapping}} = (q^{-1}C_{\text{ox}}\Delta V_{\text{max}}\sigma_0^\beta) \times Q_{\text{injected}}^{\beta-1}$$

As $\beta < 1$, the charge trapping efficiency (η_{trapping}) will decrease with a power law dependence on the injected charge density (Q_{injected}) at the initial stage of stressing.

Appendix V: J-V Characteristics of the FGA

Temperature Series Sample Set

Appendix V presents the supplementary data for the discussions in chapter 5. The plots below represent the J-V characteristics for the Au/Ni/HfO₂(8nm)/In_{0.53}Ga_{0.47}As and Au/Ni/Al₂O₃(8nm)/In_{0.53}Ga_{0.47}As MOS capacitors treated with the FGA temperature series. The main discussions can be found in section 5.3.1.

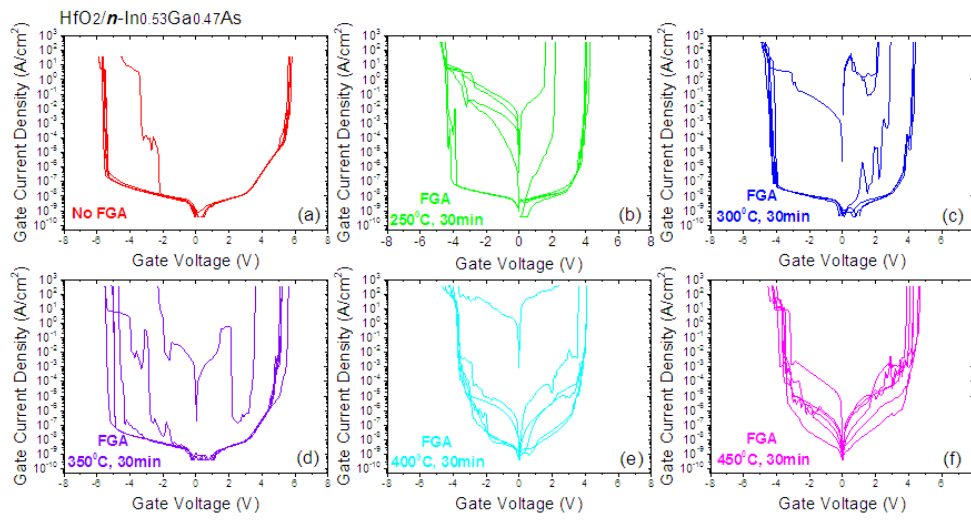


Figure V-1: J-V characteristics for Au/Ni/HfO₂(8nm)/n-In_{0.53}Ga_{0.47}As MOS capacitors treated by the FGA temperature series.

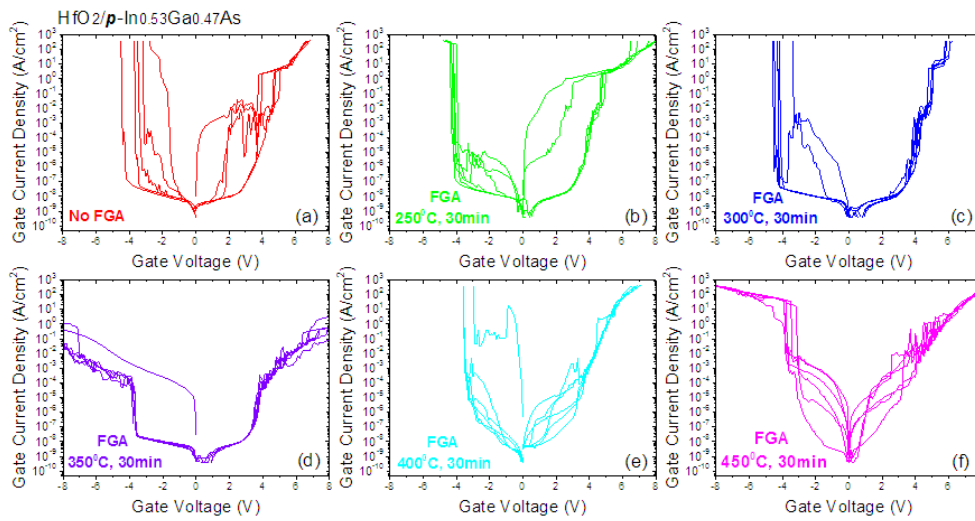


Figure V-2: J-V characteristics for Au/Ni/HfO₂(8nm)/p-In_{0.53}Ga_{0.47}As MOS capacitors treated by the FGA temperature series.

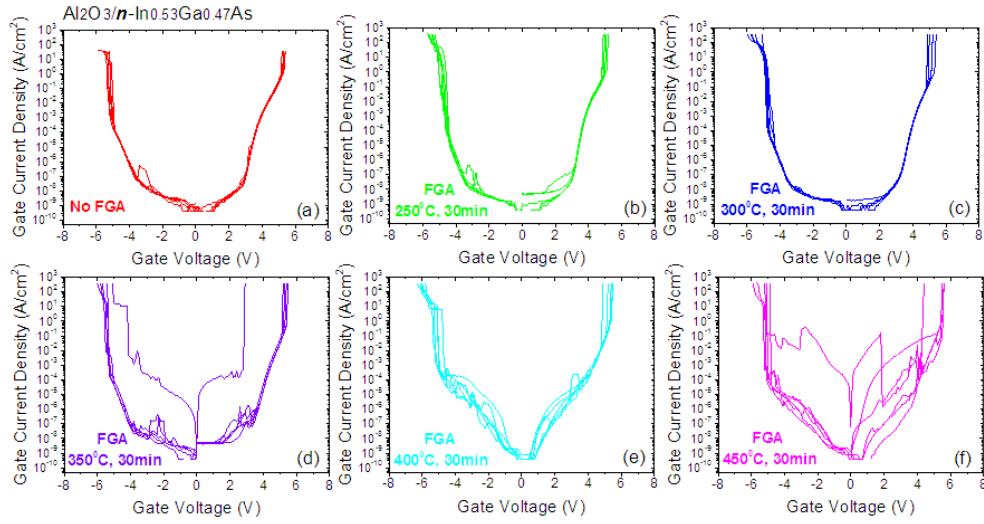


Figure V-3: J-V characteristics for Au/Ni/Al₂O₃(8nm)/n-In_{0.53}Ga_{0.47}As MOS capacitors treated by the FGA temperature series.

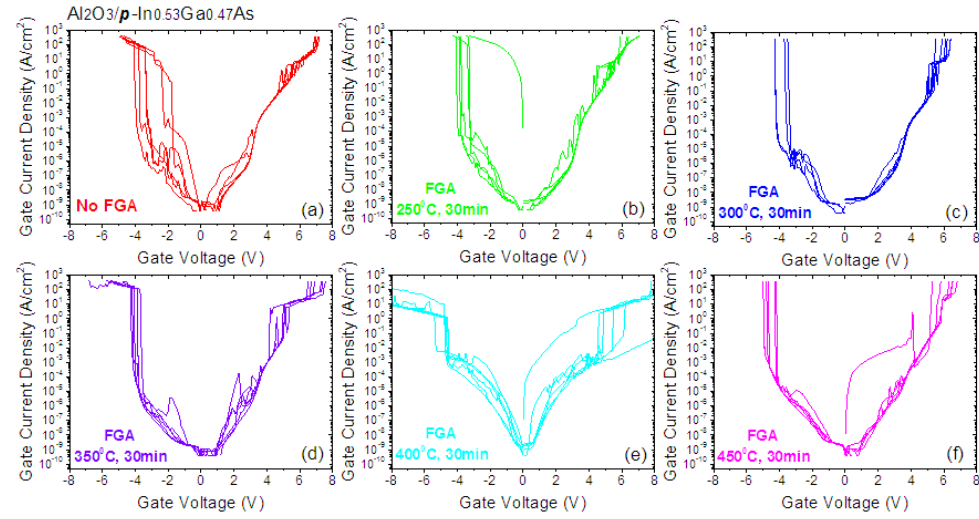


Figure V-4: J-V characteristics for Au/Ni/Al₂O₃(8nm)/p-In_{0.53}Ga_{0.47}As MOS capacitors treated by the FGA temperature series.

Appendix VI: Combined C-V and HAXPES Study of SiO₂/Si and Al₂O₃/GaAs MOS Systems

Combined C-V and HAXPES study was carried out in collaboration with Dr. Lee Walsh and Prof. Greg Hughes from Dublin City University. This work was performed on MOS systems which demonstrate efficient Fermi level movement (SiO₂/Si), partial Fermi level pinning (Al₂O₃/In_{0.53}Ga_{0.47}As) and strong Fermi level pinning (Al₂O₃/GaAs). Discussions on C-V and HAXPES of Al₂O₃/In_{0.53}Ga_{0.47}As MOS systems are presented in chapter 6. This appendix presents the papers that are published for the combined C-V and HAXPES study on Si/SiO₂ and Al₂O₃/GaAs MOS systems, which are supplementary information for chapter 6. For all MOS systems under investigation, a good agreement of Fermi level position has been achieved between the two techniques.

A combined hard x-ray photoelectron spectroscopy and electrical characterisation study of metal/SiO₂/Si(100) metal-oxide-semiconductor structures

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Combined hard x-ray photoelectron spectroscopy (HAXPES) and electrical characterisation measurements on identical Si based metal-oxide-semiconductor structures have been performed. The results obtained indicate that surface potential changes at the Si/SiO₂ interface due to the presence of a thin Al or Ni gate layer can be detected with HAXPES. Changes in the Si/SiO₂ band bending at zero gate voltage and the flat band voltage for the case of Al and Ni gate layers derived from the silicon core levels shifts observed in the HAXPES spectra are in agreement with values derived from capacitance-voltage measurements. © 2012 American Institute of Physics.

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Hard x-ray photoelectron spectroscopy (HAXPES) is emerging as a technique which has the capability of providing chemical and electronic information on much larger depth scales than conventional x-ray photoelectron spectroscopy.^{1–3} This has potential application in the study of buried interfaces as found at the oxide/semiconductor interface, particularly if changes at this interface are of interest following the subsequent deposition of a metal capping layer in the fabrication of metal-oxide-semiconductor (MOS) structures. Photoemission sampling depths in excess of 10 nm (Ref. 4) allow for direct comparison between results obtained from electrical characterisation techniques and photoemission experiments, as these measurements can be made on identical structures thereby bridging the gap between interface chemistry and electrical properties at buried interfaces.

For this study exploring the combination of HAXPES and electrical characterisation techniques, the experiments were performed on Si(100)/SiO₂ MOS structures. This system was selected as the interpretation of the multi-frequency capacitance-voltage (CV) response is well developed,⁵ the interface is representative of an unpinned surface Fermi level, and the structure allows accurate determination (± 50 meV (Ref. 6)) of surface potential for a given gate voltage based on CV measurements. The samples were formed over *n* and *p*-doped silicon substrates and were capped with high (Ni) and low (Al) work function metals to induce surface potential shifts at the Si(100)/SiO₂ interface for examination by the HAXPES and CV methods. Using a photon energy of 4150 eV in these investigations allowed for the simultaneous detection of photoemission signals from metal, oxide, and substrate core levels. The band gap of Si (1.1 eV) is wide enough to allow differences in the binding energy (BE) of the *n* and *p*-doped substrate core levels to be detected, which directly reflect different Fermi level positions in the band gap.⁷

In this paper, we illustrate the ability of HAXPES to measure Fermi level movements in the semiconductor substrate and potential differences across the oxide for MOS

structures, and explain how these results compare with CV measurements on identical structures.

High quality thermally grown SiO₂ layers, with a thickness of 8 nm, were grown using a dry oxidation process in a furnace at 850 °C on both *n* (2–4 Ω cm, $\sim 1 \times 10^{15}$ cm⁻³) and *p* (10–20 Ω cm, $\sim 1 \times 10^{15}$ cm⁻³) doped silicon(100) substrates following a standard silicon surface clean. The samples for HAXPES analysis were capped with 5 nm Ni or 5 nm Al blanket films by electron beam evaporation. For electrical characterisation, Ni/Au (90 nm/70 nm) and Al (160 nm) gate electrodes were formed by electron beam evaporation and a lift off lithography process. The Si/SiO₂ samples did not receive a final forming gas (H₂/N₂) anneal.

HAXPES work is usually performed at synchrotron radiation sources due to the need for high brilliance to compensate for the rapid decrease in subshell photo-ionization cross-section with increasing excitation energy.⁸ HAXPES measurements were carried out on the NIST beamline X24A at the National Synchrotron Light Source (NSLS) at Brookhaven National laboratory (BNL). A double Si(111) crystal monochromator allowed for photon energy selection in the range of 2.1–5.0 keV. An electron energy analyser was operated at a pass energy of 200 eV giving an overall instrumental energy resolution of ~ 0.35 eV at the chosen photon energy of 4150 eV. Samples were fixed on a grounded Al sample holder with stainless steel clips, which connected the front of the samples to the sample holder. In order to ensure correct energy calibration throughout the experiment, metallic Ni Fermi edge reference spectra were acquired immediately before and after the acquisition of the SiO₂ and Si substrate core level peaks. The resultant error associated with this photon energy correction procedure is estimated to be no more than ± 50 meV. The maximum depletion region width for the 1×10^{15} cm⁻³ doped Si substrate is ~ 800 nm and the total sampling depth of the HAXPES measurements is estimated to be no more than 23 nm (Ref. 9) for the substrate Si 1s which has a kinetic energy of ~ 2310.5 eV for the 4150 eV photon energy used in these studies,¹⁰ where the

total sampling depth includes the ability to detect the whole of the 5 nm of metal, 8 nm of oxide, and no more than 10 nm sampling depth into the Si. Therefore, the BE of the acquired Si substrate core level peaks directly reflect the position of the Fermi level in the silicon at the Si/SiO₂ interface, i.e., the surface Fermi level position. However, it is noted that for Si samples in inversion, which exhibit strong surface band bending, the sampling depth of the HAXPES may cause the peaks to shift by up to 0.1 eV to lower BE.¹¹ The CV measurements were recorded using a CV enabled meter following open calibration. The measurements were performed on-wafer at room temperature (22 °C) in a probe station in a dry air environment (dew point ≤ -65 °C).

Figure 1 shows the Si 1s core level spectra originating from the substrate and the 8 nm SiO₂ layer for both *n* and *p*-doped Si, with and without the presence of a metal gate. The BE positions of the core level peaks are measured and the difference between the *n* and *p* type Si substrates is used to estimate the Fermi level separation at the Si/SiO₂ interface. HAXPES measurements on the uncapped Si/SiO₂ samples revealed that the BE position for the *p*-type Si peaks was ~ 0.32 eV lower than the *n*-type substrate consistent with the Fermi level residing closer to the valence band edge for *p* type and closer to the conduction band edge for *n* type. The difference is however less than the expected value of 0.57 eV, which is calculated from the theoretical Fermi level position difference for *n* and *p* silicon with a doping concentration of $1 \times 10^{15} \text{ cm}^{-3}$.⁴

The reduction in measured difference in the Si 1s core level BE indicates that there is band bending present at the SiO₂/Si interface even in the absence of a metal overlayer. In order to establish the approximate position of the Fermi level in the band gap with respect to the valence band edge prior to metal deposition, valence band spectra were acquired at the same photon energy. An extrapolation of the Si valence band to a zero signal intensity yields the approximate

position of the valence band edge.¹² Although more accurate methods have been recently employed,¹³ this method is sufficient to provide the accuracy required here. Reference spectra of a sample with a Ni gate were subsequently taken, and the nickel metallic edge was used to establish the Fermi level position at 0 eV BE on the x-axis. These measurements show that the Fermi level of the *n*-type sample is ~ 0.95 eV above the valence band edge, indicating an accumulated surface with the surface Fermi level above its flat band position of 0.85 eV above the valence band. Similar measurements for the *p*-type sample show the Fermi level is ~ 0.66 eV above the valence band edge, above its flat band position of 0.28 eV, indicating that the *p*-type surface is weakly inverted. Both of these observations are consistent with fixed positive charge in the SiO₂ which is expected based on the oxidation temperature of 850 °C and the absence of any post deposition annealing.¹⁴

The effect of the deposition of high (Ni—5.15 eV (Ref. 15)) and low (Al—4.1 eV (Ref. 15)) work function metals (5 nm) on the SiO₂ surface on the Si 1s binding energy is also shown in Figure 1. If the Fermi level at the SiO₂/Si interface is free to move, it would be expected to align with the metal Fermi levels resulting in a slight increase in band bending (increase in core level BE) for the *n*-type substrate with the low work function Al contact, given that the electron affinity of Si is 4.05 eV. For the Ni contact, a large increase in band bending (reduction in core level BE) would occur as Ni has a high work function. Alternatively, for the *p*-type substrate, an Al contact would result in an increase in band bending (increase in core level BE), while a Ni contact would result in a decrease in band bending (decrease in core level BE). HAXPES measurements in Figure 1 for samples with Al gates show that the Si 1s signal originating from the silicon substrate, located at a BE of 1839 eV, shifts 0.14 eV for the *p*-type, and 0.08 eV for the *n*-type to higher BE. While for the Ni gate, the Si 1s peak shifts ~ 0.12 eV for the *p*-type and ~ 0.22 eV for the *n*-type to lower BE energy. The experimentally observed shifts for the samples with metal gates are therefore consistent with the direction of expected surface Fermi level movement, while not matching the expected shift magnitudes.

The limited ability to move the Fermi level closer to the valence band edge with the high work function Ni is consistent with fixed positive charge in the SiO₂ which will tend to accumulate electrons at the Si/SiO₂ interface. In addition, as the samples received no final forming gas (H₂/N₂) anneal, it is expected that interface defects originating from silicon dangling bonds (P_b centres) will be present, which will also restrict somewhat the movement of the surface Fermi level. The P_b centres at the Si(100)/SiO₂ interface have levels in both the lower and upper energy gap regions.^{16–18}

Work function differences between the metal and the partially pinned Si Fermi level should also result in a potential difference across the oxide layer which should manifest as a BE shift of the associated oxide core levels.^{3,7} These changes would be expected to be most apparent between the *n*-type Si and the Ni, or the *p*-type Si and the Al, as these both represent the largest difference in work functions. The spectra in Figure 1 also show the changes in BE of the Si 1s

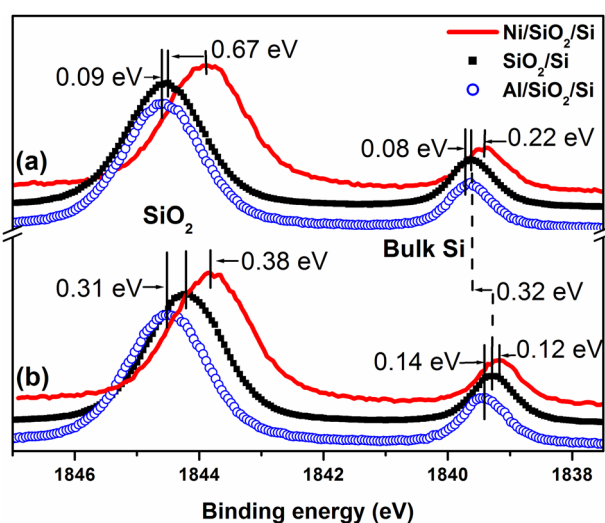


FIG. 1. Normalised Si 1s core level spectra acquired at a photon energy of 4150 eV for the uncapped Si/SiO₂, Ni (5 nm) capped Si/SiO₂ and Al (5 nm) capped Si/SiO₂ samples, showing the shifts in the core level after metal deposition and the changes in the potential across the SiO₂ layer cause by different work function metals for (a) *n*-type, and (b) *p*-type Si substrates. The dotted lines show the energy separation between *n* and *p* type samples without metal gates.

oxide peak (located at ~ 1844 eV) for both dopant types resulting from metal deposition. For a *p*-type sample the deposition of the low work function Al results in an increase in the Si 1s oxide peak BE of 0.31 eV reflecting a potential decrease consistent with the alignment of the Fermi levels. For the Ni capped *p*-type sample, a decrease in the BE of 0.38 eV is measured reflecting a potential increase across the oxide caused by the high work function Ni contact after Fermi level alignment. The corresponding BE shift for the *n*-type sample was 0.09 eV to higher BE, and 0.67 eV to lower BE for the Al and Ni cap, respectively. All of these changes are consistent with the expected polarity of the potential difference across the oxide layer caused by the low and high work function metals. Figures 2(a) and 2(b) show a schematic diagram illustrating the changes in BE due to Fermi level movements and changes in the potential field across the oxide for a *p*-type Si substrate following the deposition of Al and Ni contacts, respectively. The centre of the Si 1s oxide peak is located at a weighted average of the photoemission signal intensity from the different depths into the oxide.³ Note that the shift resulting from Fermi level movement in the bulk Si is also present in the oxide peaks, so any shift in the oxide peaks is a combination of the Fermi level movement and a potential difference across the oxide.

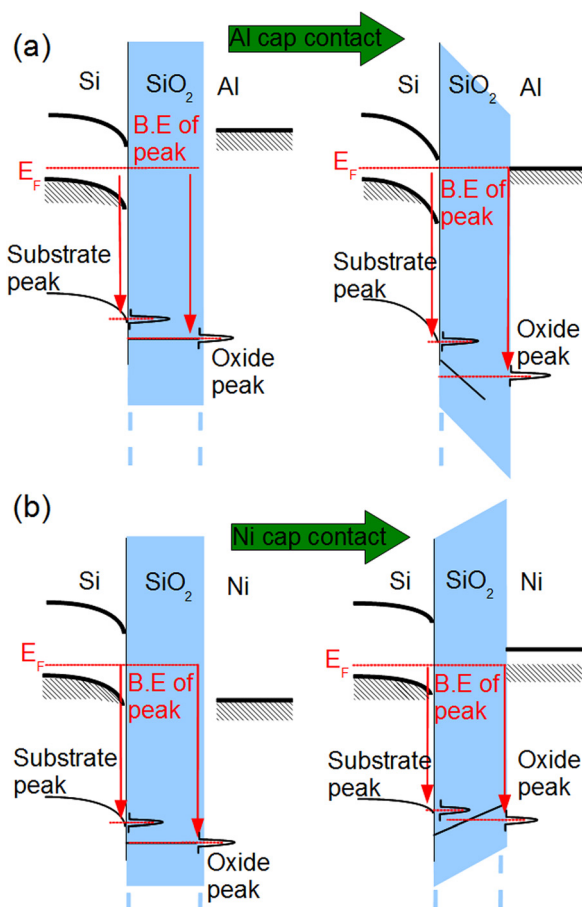


FIG. 2. (a) Band diagram illustrating the BE shifts due to an electric field across the oxide caused by metal deposition, for *p*-type Si showing a potential difference across the oxide for a *p*-type sample with an Al gate. (b) Band diagram showing a potential difference of the opposite polarity for a *p*-type sample with a Ni gate.

The CV responses recorded at an ac signal frequency of 1 MHz for the corresponding Al (160 nm) and Ni/Au (160 nm) gate Si/SiO₂ MOS capacitors for the *n* and *p*-type silicon are shown in Figures 3(a) and 3(b), respectively. The multi-frequency CV responses from 1 kHz to 1 MHz (not shown) exhibit the features associated with P_b defects at the Si/SiO₂ interface, consistent with previous publications.¹⁷ The presence of unpassivated silicon dangling bonds (P_b defects) is expected as the samples did not receive a final forming gas anneal. The ac signal frequency of 1 MHz, shown in Figures 3(a) and 3(b), was selected to minimise the effect of the silicon dangling bond defects on the CV response. Considering first the surface potential at 0 V, which is the condition for the HAXPES measurements, the CV observations match the expected results, and are consistent with the HAXPES measurements, indicating: surface accumulation for the Al gate over the *n*-type, inversion of the surface for the Al gate over *p*-type, and depletion of the surface for the Ni gate over both *n* and *p*-types. From the CV responses, the surface potential at 0 V can also be calculated by fitting the CV with a Poisson CV solver.^{19,20} From the resulting surface potentials (Φ_s), the values of E_F-E_v at 0 V are shown in Figure 3, and compared with the corresponding HAXPES measurements in Table I. The shift in surface potential for the Al with respect to the Ni gate samples on

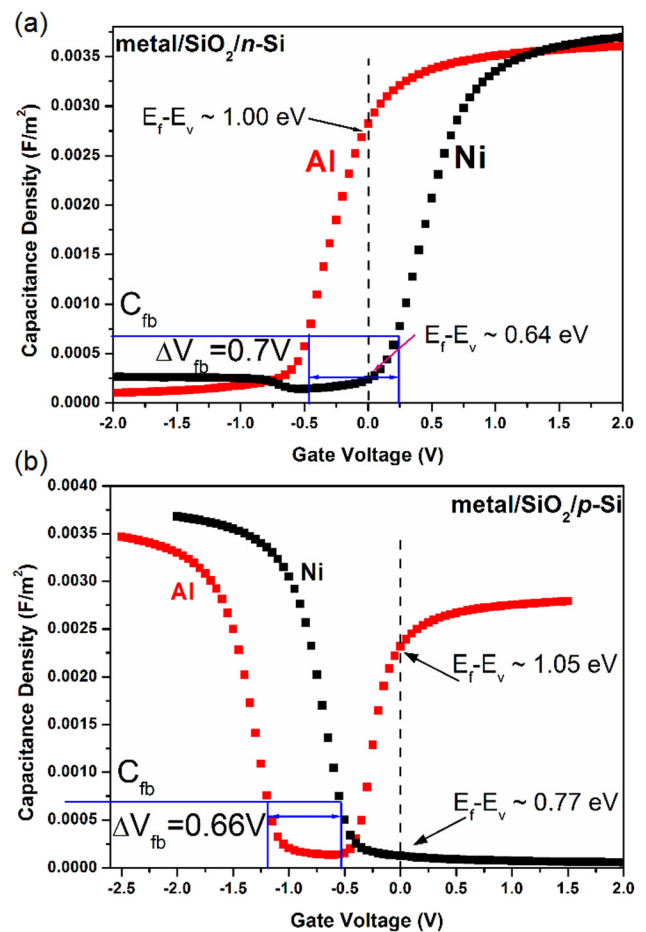


FIG. 3. CV characteristics (1 MHz) for the metal/SiO₂/Si samples with Al and Ni gates for both (a) *n*-type, and (b) *p*-type substrates, displaying both the flat band shifts ΔV_{fb} and the calculated surface Fermi level (E_F) position at zero gate voltage. The Fermi level position is with respect to the valence band (E_F-E_v).

TABLE I. Summary of the HAXPES and CV results.

Sample	E_F-E_v (SiO ₂ /Si)	E_F-E_v (Al/SiO ₂ /Si)	E_F-E_v (Ni/SiO ₂ /Si)	ΔE_F (Al-Ni shift)	Flat band (Al-Ni shift)
<i>n</i> -type (CV)	N/a	1.00 eV	0.64 eV	0.36 eV	0.7 V
<i>n</i> -type (HAXPES)	0.95 eV	1.03 eV	0.73 eV	0.3 eV	0.76 eV
<i>p</i> -type (CV)	N/a	1.05 eV	0.77 eV	0.28 eV	0.66 V
<i>p</i> -type (HAXPES)	0.66 eV	0.8 eV	0.54 eV	0.26 eV	0.69 eV

n-type silicon is 0.36 eV which compares to the value of 0.3 eV from HAXPES. For the *p*-type sample the surface potential shift from the Al to the Ni gate is 0.28 eV which compares to 0.26 eV from the HAXPES as shown in Table I. When taking into account the errors in surface potential for the two methods which are ± 50 meV for both the HAXPES and CV fitting, this is a good agreement between the HAXPES and CV analysis. The increase in capacitance observed in Figure 3(b) for the *p*-type Al/SiO₂/Si MOS structure at positive gate bias is attributed to peripheral inversion effects.²¹

As well as providing information on the surface potential at zero gate voltage, the HAXPES method can also detect the flat band voltage difference between the Ni and Al gate samples. The flat band voltage in a MOS capacitor is the gate voltage required to offset the built in potential, which is across the oxide and the silicon substrate at 0 V, to achieve a flat band condition. As a consequence, the difference in the flat band voltage in the CV for the Ni and Al gate samples should relate to the BE shifts measured in the HAXPES Si 1s oxide signal, as these spectra include both the Fermi level shifts in the substrate and the potential difference across the oxide. The calculated flat band capacitance (C_{fb}) is indicated in Figures 3(a) and 3(b), and the flat band voltage difference for the Al and Ni gate samples is 0.7 V for the *n*-type and 0.66 V for the *p*-type. This is in very good agreement with the combined Al-Ni shifts in the Si 1s oxide spectra in Figure 1, which are 0.69 eV and 0.76 eV for the *p* and *n*-type substrates, respectively. The agreement between the surface potential differences and the flat band voltage differences for the two measurement techniques are shown in Table I. There is very good agreement in the relative shifts between samples with Al and Ni gates, however, there is a discrepancy between the *p*-type Fermi level positions determined by the two techniques. The results in Figure 3 provide a possible explanation. The *p* type samples are either at the onset of strong inversion (Ni) or in strong inversion (Al) at 0 V and consequently have larger surface band bending than the *n* type samples which are in depletion (Ni) or slight accumulation (Al). If we assume a maximum sampling depth into the Si substrate of 10 nm, the band-bending will vary by 0.1–0.15 eV for a *p* type sample in inversion based on a Poisson-Schrodinger simulation.¹¹ This variation would be apparent in the HAXPES measurement resulting in a lower E_F-E_v than obtained from the CV analysis.

In conclusion, the large sampling depth of HAXPES has been exploited to characterise band bending in metal/SiO₂/Si

MOS structures fabricated with both high (Ni) and low (Al) work function metals. The HAXPES measurements of the Si 1s core level have been shown to be sensitive to changes in band bending at the Si/SiO₂ interface due to the presence of high (Ni) and low (Al) work function metals. The Si 1s core level originating from the SiO₂ layer indicates the presence of a potential difference across the SiO₂ layer. The changes in the band bending at the Si/SiO₂ interface and the potential difference across the SiO₂ are consistent with the difference in metal work functions and are in agreement with the results derived from CV measurements.

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- ¹K. Kobayashi, M. Yabashi, Y. Takata, T. Tokushima, S. Shin, K. Tamasaku, D. Miwa, T. Ishikawa, H. Nohira, T. Hattori, Y. Sugita, O. Nakatsuka, A. Sakai, and S. Zaima, *Appl. Phys. Lett.* **83**, 1005 (2003).
- ²P. S. Lysaght, J. Barnett, G. I. Bersuker, J. C. Woicik, D. A. Fischer, B. Foran, H.-H. Tseng, and R. Jammy, *J. Appl. Phys.* **101**, 024105 (2007).
- ³K. Kakushima, K. Okamoto, K. Tachi, J. Song, S. Sato, T. Kawanago, K. Tsutsui, N. Sugii, P. Ahmet, T. Hattori, and H. Iwai, *J. Appl. Phys.* **104**, 104908 (2008).
- ⁴R. Claessen, M. Sing, M. Paul, G. Berner, A. Wetscherek, A. Müller, and W. Drube, *New J. Phys.* **11**, 125007 (2009).
- ⁵E. H. Nicollian and J. R. Brews, *MOS Physics and Technology* (Wiley, New York, 2003).
- ⁶M. J. Uren, J. H. Stathis, and E. Cartier, *J. Appl. Phys.* **80**, 3915 (1996).
- ⁷C. C. Fulton, G. Lucovsky, and R. J. Nemanich, *J. Appl. Phys.* **99**, 063708 (2006).
- ⁸J. J. Yeh and I. Lindau, *At. Data Nucl. Data Tables* **32**, 1 (1985).
- ⁹S. Tanuma, T. Shiratori, T. Kimura, K. Goto, S. Ichimura, and C. J. Powell, *Surf. Interface Anal.* **37**, 833 (2005).
- ¹⁰J. F. Moulder and J. Chastain, *Handbook of X-Ray Photoelectron Spectroscopy: A Reference Book of Standard Spectra for Identification and Interpretation of XPS Data* (Eden Prairie, Perkin-Elmer Corp., 1992).
- ¹¹T. P. O'Regan, P. K. Hurley, B. Soree, and M. V. Fischetti, *Appl. Phys. Lett.* **96**, 213514 (2010).
- ¹²A. Bahari, P. Morgen, and Z. S. Li, *Surf. Sci.* **600**, 2966 (2006).
- ¹³M. Gaowei, E. M. Muller, A. K. Rumaiz, C. Weiland, E. Cockayne, J. Jordan-Sweet, J. Smedley, and J. C. Woicik, *Appl. Phys. Lett.* **100**, 201606 (2012).
- ¹⁴B. E. Deal, M. Sklar, A. S. Grove, and E. H. Snow, *J. Electrochem. Soc.* **114**, 266 (1967).
- ¹⁵D. R. Lide, *CRC Handbook of Chemistry and Physics* (CRC, Boca Raton, 2007).
- ¹⁶L.-A. Ragnarsson and P. Lundgren, *J. Appl. Phys.* **88**, 938 (2000).
- ¹⁷K. Keunen, A. Stesmans, and V. V. Afanas'ev, *Phys. Rev. B* **84**, 085329 (2011).
- ¹⁸G. J. Gerardi, E. H. Poindexter, M. E. Rueckel, P. J. Caplan, and N. M. Johnson, *Appl. Phys. Lett.* **49**, 348 (1986).
- ¹⁹J. R. Hauser and K. Ahmed, *AIP Conf. Proc.* **449**, 235 (1998).
- ²⁰F. Lime, C. Guiducci, R. Clerc, G. Ghibaudo, C. Leroux, and T. Ernst, *Solid-State Electron.* **47**, 1147 (2003).
- ²¹E. O'Connor, K. Cherkaoui, S. Monaghan, D. O'Connell, I. Povey, P. Casey, S. B. Newcomb, Y. Y. Gomeniuk, G. Provenzano, F. Crupi, G. Hughes, and P. K. Hurley, *J. Appl. Phys.* **111**, 124104 (2012).

Hard x-ray photoelectron spectroscopy and electrical characterization study of the surface potential in metal/Al₂O₃/GaAs(100) metal-oxide-semiconductor structures

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Hard x-ray photoelectron spectroscopy (HAXPES) has been used to study metal-oxide-semiconductor (MOS) structures fabricated with both high (Ni) and low (Al) work-function metals on 8-nm thick Al₂O₃ dielectric layers, deposited on sulfur passivated *n*- and *p*-doped GaAs substrates. A binding energy difference of 0.6 eV was measured between the GaAs core levels of the *n*- and *p*-doped substrates in the absence of gate metals, indicating different Fermi level positions in the band gap. Subsequent photoemission measurements made on the MOS structures with the different work-function metals displayed very limited change in the GaAs core level binding energies, indicating that the movement of the Fermi level at the Al₂O₃/GaAs interface is restricted. Using a combination of HAXPES measurements and theoretical calculations, the Fermi level positions in the band gap have been determined to be in the range of 0.4–0.75 eV and 0.8–1.11 eV above the valence band maximum for *p*- and *n*-type GaAs, respectively. Analysis of capacitance voltage (C-V) measurements on identically prepared samples yield very similar Fermi level positions at zero applied gate bias. The C-V analysis also indicates a higher interface defect density (D_{it}) in the upper half of the GaAs bandgap.

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I. INTRODUCTION

The recent increased interest in the nondestructive analysis of buried interfaces, such as those in metal oxide semiconductor (MOS) structures, has been facilitated by the development of a high energy variant of x-ray photoelectron spectroscopy (XPS) known as hard-XPS (HAXPES). The increase in the analysis depth, from 5–7 nm for conventional XPS up to 15–30 nm for HAXPES,^{1–4} facilitates the measurement of core level signals from all the relevant layers in MOS structures which can also be electrically characterized by capacitance-voltage (C-V) techniques. The ability of HAXPES measurements to provide information on band bending at the semiconductor/dielectric interface and to detect the presence of a potential difference across the dielectric provides complementary information on the electronic structure of the MOS to that deduced from C-V measurements.⁵ This is of particular interest in cases where it is difficult to extract definitive information from conventional C-V analysis due to high interface state densities, as is the case with GaAs.⁶

In this paper we report on a study exploring the application of HAXPES analysis to determine the surface Fermi level position in *n*- and *p*-doped GaAs MOS structures, where the oxide is an Al₂O₃ (8-nm) thin film deposited by atomic layer deposition (ALD). The samples studied included Al₂O₃/GaAs structures with no metal gates and samples capped with 5-nm thick high (Ni) and low (Al) work-function metals, to explore

if the low and high work-function metal layers modulate the surface Fermi level position. Using a photon energy of 4150 eV in these investigations allowed the detection of photoemission signals from metal, oxide, and substrate core levels. The relatively wide band gap of GaAs (1.42 eV) increases the possibility of detecting differences in the binding energy (BE) of the *n*- and *p*-doped substrate core levels which directly reflect different Fermi level positions in the band gap.⁷ The surface Fermi level positions obtained from the HAXPES analysis are compared to the reported location of the pinning positions in the GaAs band gap for *n*- and *p*-doped substrates from other studies.^{8–10}

In conjunction with the HAXPES analysis, Al₂O₃/GaAs MOS samples with *n*- and *p*-doped GaAs substrates and Ni or Al gate contacts were examined using C-V analysis. The GaAs/oxide interface is known to display capacitance-voltage characteristics in MOS devices indicative of a high density of interface states, which restricts the movement of the Fermi level at the GaAs/oxide interface upon application of a gate voltage. To fully characterize the interfacial electronic properties in the high- κ /GaAs MOS system it is necessary to determine the energy distribution of the interface states. In the case of an MOS system with a high interface state density, such as GaAs, the conversion of the gate voltage in the C-V response to the corresponding energy position in the interface state analysis is an established problem.¹¹ It would be highly beneficial to the community working in the electrical characterization of III-V MOS interface states

to have an independent method of evaluating the surface potential for a given gate voltage, as this would provide a higher degree of certainty for energy mapping of the interface states.

The results presented in this paper illustrate the ability of HAXPES to detect Fermi level positions at the GaAs/dielectric interface, and the presence of any potential differences across the dielectric layers. The results from the HAXPES analysis are also compared to the analysis of the C-V response, and a good agreement is obtained for the surface Fermi level position for the case of zero applied gate voltage (V_g).

II. EXPERIMENTAL

The n - (Si, $5 \times 10^{17} \text{ cm}^{-3}$) and p - (Zn, $5 \times 10^{17} \text{ cm}^{-3}$) doped GaAs samples consisted of 400-nm thick GaAs layers grown by metal organic vapor-phase epitaxy (MOVPE) on epi-ready GaAs substrates. The samples received a surface treatment using a 10% solution of $(\text{NH}_4)_2\text{S}$ in deionized water for 20 min at room temperature immediately prior to being transferred into the ALD chamber with less than 3 min air exposure.¹² The 8-nm Al_2O_3 was deposited by ALD at 300 °C using alternating TMA ($\text{Al}(\text{CH}_3)_3$) and H_2O pulses. The samples were split into three groups: A, B, and C, each containing one n - and one p -type GaAs sample. Group A was left without a metal gate, group B was capped with a 5-nm Ni blanket film, while group C was capped with a 5-nm Al blanket film. All metal deposition was achieved by electron beam evaporation. Additionally, two further groups, D and E were produced for C-V analysis in an identical fashion to that mentioned above, with group D samples capped with a 160-nm Al film, while group E samples were capped with a 70/90 nm Ni/Au film for electrical probing. The metal gate areas for the C-V characterization were defined by a lithography and lift-off process.

HAXPES measurements were carried out on the NIST beamline X24A at the National Synchrotron Light Source (NSLS) at Brookhaven National laboratory (BNL). A double Si (111) crystal monochromator allowed for photon energy selection in the range of 2.1–5.0 keV. An electron energy analyzer was operated at a pass energy of 200 eV giving an overall instrumental energy resolution of 0.52 eV at the chosen photon energy of 4150 eV. In order to ensure correct energy calibration throughout the experiment, metallic Ni Fermi edge reference spectra were acquired immediately before and after the acquisition of the Al_2O_3 and GaAs substrate core level peaks. The resultant error associated with this photon energy correction procedure is estimated to be no more than 50 meV. The maximum depletion region width for the $5 \times 10^{17} \text{ cm}^{-3}$ doped GaAs substrate is calculated to be 61 nm. The total sampling depth of the HAXPES measurement using a photon energy of 4150 eV is estimated to be 23 nm¹³ which ensures the detection of photoemitted electrons from the 5-nm metal and 8-nm dielectric layers, as well as approximately 10 nm into the GaAs, which is obtained from the inelastic mean free path of the As 2*p* photoemitted electrons, which have kinetic energies of 2827 eV.¹⁴ The XPS core level spectra were curve fitted, using Voigt profiles composed of Gaussian and Lorentzian line shapes in a 3:1 ratio with a Shirley-type background, to increase the accuracy of locating the peak centers.

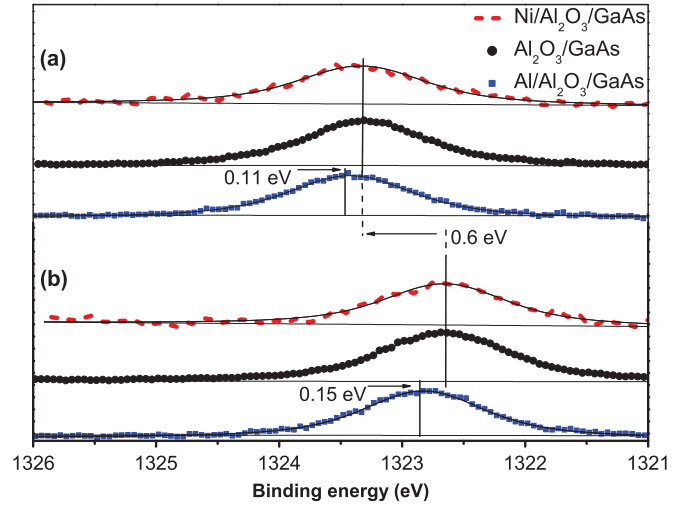


FIG. 1. (Color online) Normalized As 2*p* core level spectra acquired at a photon energy of 4150 eV for the uncapped $\text{Al}_2\text{O}_3/\text{GaAs}$, Ni (5 nm) capped and Al (5 nm) capped $\text{Al}_2\text{O}_3/\text{GaAs}$ samples, showing the shifts in the core level after metal for (a) n -type, and (b) p -type GaAs substrates. The dotted lines show the energy separation between n - and p -type samples without metal gates.

III. RESULTS AND DISCUSSION

Figure 1 shows the As 2*p* core levels acquired at 4150 eV photon energy for both n - and p -doped GaAs with the 8-nm Al_2O_3 dielectric layer, with and without the presence of a metal overlayer. Measurements on the uncapped samples reveal that the binding energy position for the p -type GaAs peaks was found to be 0.6 eV lower than the n -type substrate consistent with the Fermi level residing closer to the valence band maximum. The difference is however less than the expected value of 1.34 eV, which is based on the calculated Fermi level position difference for n and p GaAs with a doping concentration of $5 \times 10^{17} \text{ cm}^{-3}$, indicating that there is band bending at the $\text{Al}_2\text{O}_3/\text{GaAs}$ interface for both dopant types, even in the absence of a metal contact.¹⁵

In order to determine whether the band bending displayed at the interface reflected Fermi level pinning, both high (Ni 5.01 eV) and low (Al 4.08 eV) work-function metal films 5-nm thick were deposited on the dielectric.¹⁶ By ensuring electrical contact between the metal overlayer and the GaAs substrate, Fermi level equalization across the MOS structure resulting from the differences in work functions occurs. If the Fermi level at the $\text{Al}_2\text{O}_3/\text{GaAs}$ interface is free to move, it would be expected to align with the metal work function resulting in a reduction in band bending (increase in core level binding energy) for the n -type substrate with the low work-function Al contact and an increase in the band-bending (reduction in core level binding energy) for the high work-function Ni contact. The same dependence of core level binding energy on metal work function would be expected for the p -type substrate, however, the magnitude of the shifts would differ, so for an Ni gate a much larger core level binding energy shift should be recorded for n type than for p type, while for an Al gate we would expect a larger shift for p type than for n type.

HAXPES measurements for samples with an Al gate show that the peaks shift 0.11 eV and 0.15 eV to higher BE, for

n- and *p*-type samples, respectively, with no detectable change for the Ni gate. The limited ability to move the Fermi level of either dopant type suggests high D_{it} at the $\text{Al}_2\text{O}_3/\text{GaAs}$ interface. The small shift in the GaAs core levels following the deposition of the low work-function Al contact indicates that there is a limited ability of the Fermi level to move towards the conduction band. These combined results indicate that the band bending observed at the $\text{Al}_2\text{O}_3/\text{GaAs}$ interface for the *n*- and *p*-doped substrates in the absence of a metal contact broadly reflects the position of the partially pinned Fermi level, as no significant Fermi level movements occurred following the deposition of metals with different work functions. The measurements also suggest that the partial Fermi level pinning for *n*- and *p*-doped substrates at different positions in the band gap are caused by different interface state defects consistent with previous studies.^{9,17,18} This result is in agreement with the recent work of Caymax *et al.*⁹ for electrical measurements on sulfur treated $\text{Al}_2\text{O}_3/\text{GaAs}$ MOS capacitors on *n*- and *p*-doped substrates which reported different defect state distributions in the GaAs band gap and the limited ability of sulfur treatment to passivate the mid-gap defect states. The reduction in signal to noise apparent in the spectra for the GaAs substrate peaks following the metal deposition reflects an intensity attenuation of 84% in the case of the Al contact and a 91% reduction for the Ni contact which highlights the necessity for the large sampling depth and high brilliance capabilities of HAXPES measurements.

Following the work of Kraut *et al.*,¹⁹ the position of the VBM in relation to a reference metallic Fermi level was determined by theoretically calculating the density of states (DOS) from first principles. The theoretical DOS is then weighted by the cross section of each atomic orbital, and convolved with a Gaussian curve, $\sigma = 0.5$ eV full width at half maximum, in order to accurately model the VB as measured by photoemission.²⁰ Figure 2 shows the good agreement

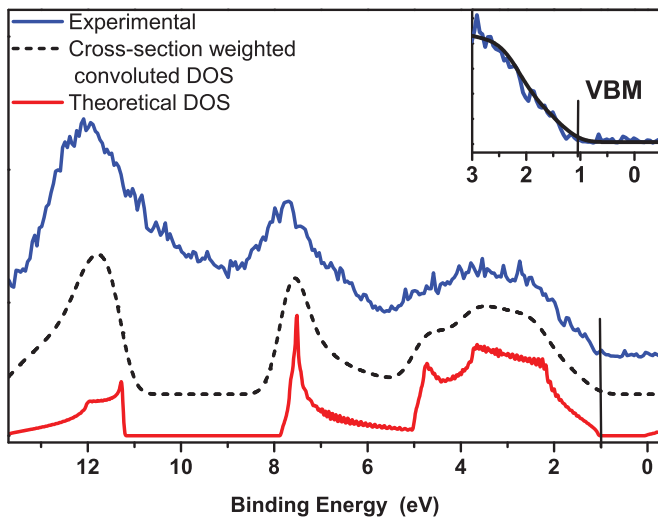


FIG. 2. (Color online) Total theoretical DOS, convolved cross section weighted DOS and experimental photoemission valence band spectra of *n*-type $\text{GaAs}/\text{Al}_2\text{O}_3$. A Gaussian of $\sigma = 0.5$ eV was used in convolution. The VBM position is indicated by the vertical line. The Ni Fermi edge was used to determine zero binding energy on this scale which reflects the Fermi level position.

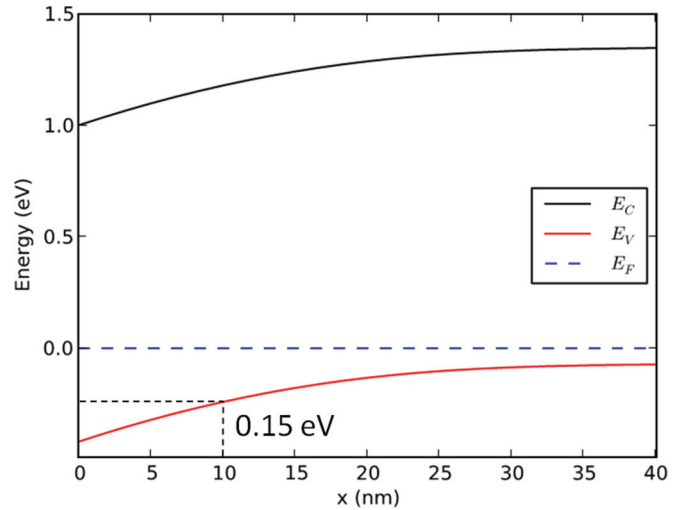


FIG. 3. (Color online) Simulation of the band bending in a *p*-type GaAs MOS structure based on 0.4-eV band bending as measured by HAXPES.

between the calculated DOS and the VB spectrum for *n*-type $\text{Al}_2\text{O}_3/\text{GaAs}$ as measured by photoemission. The VBM for this *n*-doped substrate is determined to be approximately 1.0 ± 0.1 eV below the reference Fermi level, which would be at zero binding energy on the *x* axis, while the corresponding VBM for the *p*-type $\text{Al}_2\text{O}_3/\text{GaAs}$, determined using the same method, was 0.4 ± 0.1 eV below the Fermi level.

In order to assess the magnitude of the error in determining the Fermi level position from the HAXPES measurement, a simulation of the band bending for $5 \times 10^{17} \text{ cm}^{-3}$ doped *p*-type GaAs resulting from a 0.4-eV surface potential was performed by numerically solving Poisson's equation. The resulting band-bending diagram shown in Fig. 3 indicates that for a sampling depth into the GaAs substrate of 10 nm, the error in determining the VBM position is a maximum of 0.15 eV. However, due to the exponential fall off in the weighting of the photoemitted electron contribution with depth, it would be reasonable to assume that the actual error is likely to be less than 0.1 eV. This analysis allows the determination of the Fermi level position for the *p*-type sample without a metal cap, or with an Ni cap, to be in the range of 0.4–0.5 eV above the VBM, while for the sample with the Al cap the Fermi level is 0.55–0.65 eV above the VBM. For the equivalent *n*-type sample, assuming a similar band-bending derived error, the Fermi level is in the range of 0.9–1.0 eV above the VBM for uncapped and Ni capped samples, and 1.01–1.11 eV for Al capped samples.

In order to quantify any surface photovoltage (SPV) related effect,²¹ caused by the generation of electron hole pairs in the GaAs by a high incident photon flux, the following analysis has been undertaken. SPV effects are characterized by a rigid shift of both semiconductor substrate and metal derived peaks towards the flat band positions.²¹ This has the effect on *p*-type substrates of shifting the metallic Fermi edge above the reference Fermi level by an amount equivalent to the band flattening cause by SPV, but no such shift was observed in this work. In addition, the relatively high doping density ($5 \times 10^{17} \text{ cm}^{-3}$), and the fact that measurements were

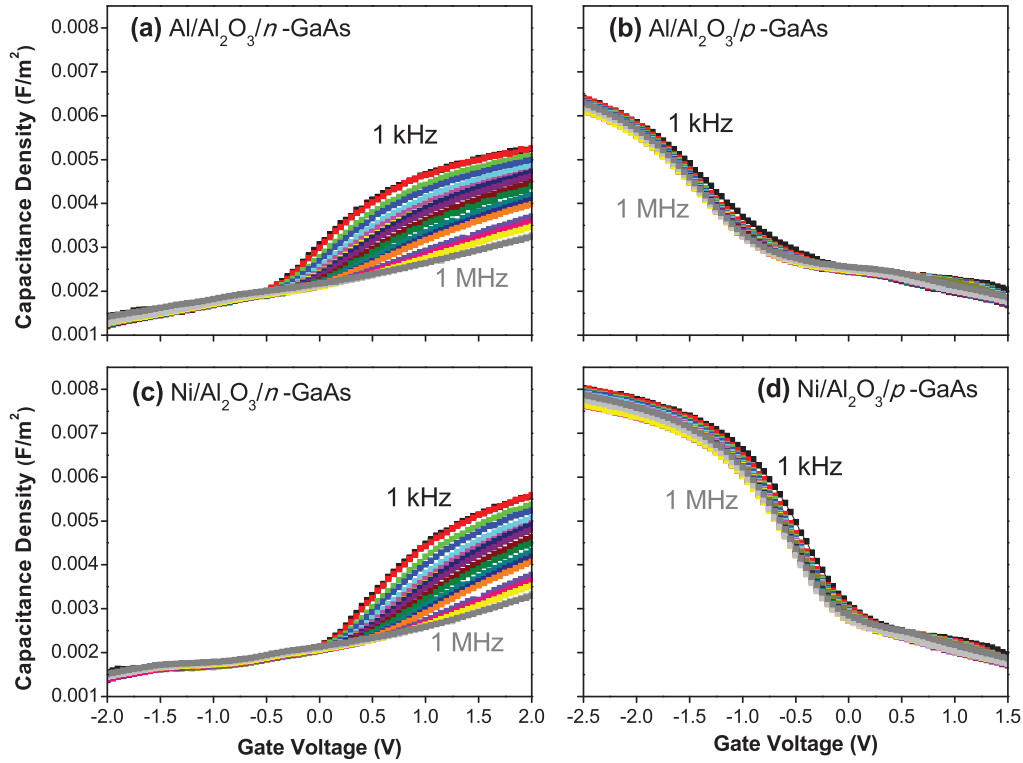


FIG. 4. (Color online) Multifrequency (1 kHz to 1 MHz) C-V response at room temperature (~ 295 K) for (a) Al/Al₂O₃/n-GaAs, (b) Al/Al₂O₃/p-GaAs, (c) Ni/Al₂O₃/n-GaAs, and (d) Ni/Al₂O₃/p-GaAs MOS capacitors.

performed at room temperature both act to minimize any SPV effect.²² Deriving similar Fermi level positions from both metal capped and uncapped samples also indicates that a significant SPV effect is not occurring, as the presence of a metal cap should act to reduce the SPV effect.²² In any case, studies by Bauer *et al.*²² would indicate that for the photon flux used in these measurements (maximum of 10^{11} photons/s) and the doping density of the GaAs substrates, an upper estimate of the SPV effect would result in no more than a 0.1-eV shift towards the flat band positions. Even taking these SPV-induced shifts into account, and adding this to the error as a result of the band bending, the results suggest that the Fermi level of the *p*-type sample is in the range 0.4–0.6 eV above the valence band maximum (VBM) for uncapped and Ni capped samples, and 0.55–0.75 eV for Al capped samples, above its calculated position of 0.04 eV above VBM. The corresponding analysis for the *n*-type Fermi level position is in the range 0.8–1.0 eV from the VBM for uncapped and Ni capped samples, and 0.91–1.11 eV for Al capped samples, below its calculated position of 1.38 eV above VBM, which agree with the *n-p* Fermi level separation of 0.6 eV as determined from the core level peak shifts. These Fermi level positions are in good agreement with those previously reported for *p*-type GaAs, 0.4–0.6 eV,⁸ and 0.33 eV²³ above the VBM. However there is a greater discrepancy in the *n*-type Fermi levels, with previous values of 0.61 eV²³ and 0.7 eV.²⁴ The presence of two pinning positions close to the midgap is, however, consistent with the unified defect model (UDM), which explains the two pinning states as being related to acceptor (missing As atom) or donorlike (missing Ga atom) states which are due to missing atoms at the semiconductor/oxide interface.^{9,25}

In order to fully characterize the presence of interface states at the dielectric-semiconductor interface, both high and low ac frequency C-V measurements are required. The C-V responses recorded at a range of ac signal frequency (1 kHz to 1 MHz) for the corresponding Al (160 nm) and Ni/Au (70/90 nm) gate GaAs/Al₂O₃ MOS capacitors for the *n*- and *p*-type GaAs are shown in Figs. 4(a)–4(d). A large frequency dispersion at positive gate voltages is observed in the C-V for the *n*-type GaAs, which is consistent with the high interface state density in the upper half of the GaAs band gap. The accumulation capacitance is not seen from the 1-MHz C-V, suggesting that the Fermi level is pinned at a fixed energy level at the Al₂O₃/GaAs interface for *n* type and cannot move towards the conduction band to accumulate electrons. The accumulationlike capacitance measured at 1 kHz is not only due to the differential capacitance (C_s) of the *n*-type GaAs but is a consequence of a capacitance contribution of an interface state capacitance (C_{it}) in parallel with C_s . As C_{it} is large compared to C_s and C_{ox} , according to the equivalent circuit of a MOSCAP with the presence of interface states,¹⁵ a capacitance that approaches C_{ox} can be observed but does not indicate that accumulation is achieved. Because the Fermi level is pinned at the fixed energy level, all the additional gate charge is compensated by charging Al₂O₃/GaAs interface defects. A similar C-V response was also observed for a HfO₂/GaAs MOS capacitor at 295 K.²⁶ The multifrequency C-V response for the *p*-type GaAs MOS capacitors shows much smaller frequency dispersion at negative gate voltages, with a maximum capacitance that approaches C_{ox} at both 1 kHz and 1 MHz, implying that the interface state density is reduced in the lower half of the GaAs band gap in comparison to the

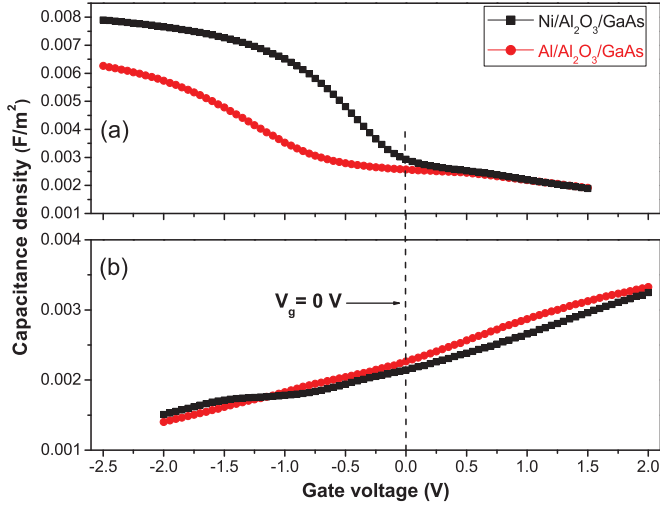


FIG. 5. (Color online) Comparison of 1-MHz C-V between Al and Ni gates for (a) *p*-GaAs and (b) *n*-GaAs.

upper half, thus the *p* type can more easily reach accumulation than the *n* type.

The work-function difference between Al and Ni on the MOS structures under investigation is estimated from the C-V at 1 MHz as shown in Figs. 5(a) and 5(b) for *p*- and *n*-type, respectively. In order to obtain the Fermi level position, the GaAs surface potential is calculated based on the measured capacitance at 1 MHz and zero gate voltage, as the HAXPES measurement is carried out without applying a gate voltage. It is crucial to do the calculation on the premise that a true high frequency capacitance is obtained at $V_g = 0$ V, otherwise the measured capacitance comprises a C_{it} term which leads to an incorrect surface potential. A model by Brammertz *et al.*⁶ that determines the interface trap response at 295 K using a capture cross section of $1 \times 10^{-14} \text{ cm}^2$ is shown in Fig. 6. It is evident that only the interface defects in the energy range E_v to $E_v + 0.31$ eV and $E_c - 0.27$ eV to E_c can respond to an ac frequency of 1 MHz. All the interface states outside this energy range will only affect the C-V through a stretch-out along the gate voltage axis without the addition of C_{it} to the total capacitance of the MOS capacitor. As discussed earlier, the HAXPES measurements indicate that the Fermi level is located in the range of 0.8–1.11 eV and 0.4–0.75 eV above the VBM for the *n* and *p* types, respectively. It is noted that these energy positions are in the region where interface states cannot respond, giving us confidence in calculating the surface potential using the 1-MHz capacitance at $V_g = 0$ V. In addition, it is worth highlighting that for GaAs, the capture cross section can vary

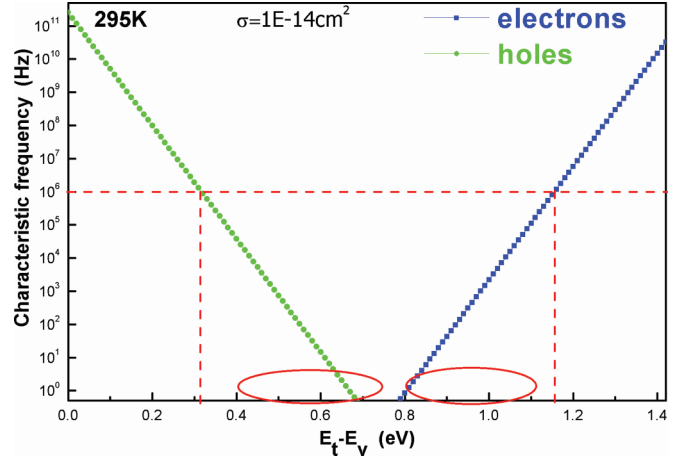


FIG. 6. (Color online) Simulation of trap response using the model by Brammertz *et al.*⁶ associated with the measurement at 295 K, assuming a capture cross section of $1 \times 10^{-14} \text{ cm}^2$. The horizontal dashed line corresponds to the high frequency of 1 MHz in the C-V measurement and circled regions represent the energy levels of interface states (E_t) in the GaAs band gap measured by HAXPES, which are in the ranges 0.8–1.11 eV and 0.4–0.75 eV above VBM for the *n* and *p* type, respectively, in the absence of metal contacts and approximately the same after the deposition of the Al or Ni gate. For smaller values of capture cross section the region of the energy gap over which the interface states can respond is reduced.

over orders of magnitude.²⁷ The calculations for the model have been performed for capture cross sections which span 3 orders of magnitude (1×10^{-17} to $1 \times 10^{-14} \text{ cm}^2$), which all show that no interface states at those energy levels can respond to 1 MHz at $V_g = 0$ V. From the C-V at 1 MHz the corresponding semiconductor depletion capacitance can be calculated from the total measured capacitance ($C_{it} = 0$) and an oxide capacitance value $C_{ox} = 9.5 \times 10^{-7} \text{ F/cm}^2$ assuming an Al_2O_3 layer with nominal thickness of 8 nm is formed during the ALD. This value can then be used to determine the surface potential and hence the surface Fermi level position with respect to the VBM. The C-V-based calculations indicate that for the *n* type the Fermi level is 0.86 eV and 0.78 eV above the VBM with Al and Ni gates, respectively, and for the *p*-type, it is 0.41 eV and 0.30 eV above the VBM with Al and Ni gates, respectively, which are in good agreement with the HAXPES measured Fermi level positions. The comparative HAXPES and C-V results ($V_g = 0$) for the surface Fermi level position are presented in Table I. The difference between the Fermi level position of Al and Ni is thus 0.08 eV over the *n* type and 0.11 eV over the *p* type, which is consistent with the Fermi level shift between Al and Ni from HAXPES over both the *n*

TABLE I. Comparison of Fermi level positions recorded by HAXPES and C-V measurements at $V_g = 0$ V. E_f is the Fermi level energy; E_v is the valence band energy.

Sample	$E_f - E_v$ ($\text{Al}_2\text{O}_3/\text{GaAs}$)	$E_f - E_v$ ($\text{Al}/\text{Al}_2\text{O}_3/\text{GaAs}$)	$E_f - E_v$ ($\text{Ni}/\text{Al}_2\text{O}_3/\text{GaAs}$)	ΔE_f (Al-Ni shift)
<i>n</i> -type (C-V)	n/a	0.86 eV	0.78 eV	0.08 eV
<i>n</i> -type (HAXPES)	0.8 – 1.0 eV	0.91 – 1.11 eV	0.8 – 1.0 eV	0.11 – 0.31 eV
<i>p</i> -type (C-V)	n/a	0.41 eV	0.30 eV	0.11 eV
<i>p</i> -type (HAXPES)	0.4 – 0.6 eV	0.55 – 0.75 eV	0.4 – 0.6 eV	0.15 – 0.35 eV

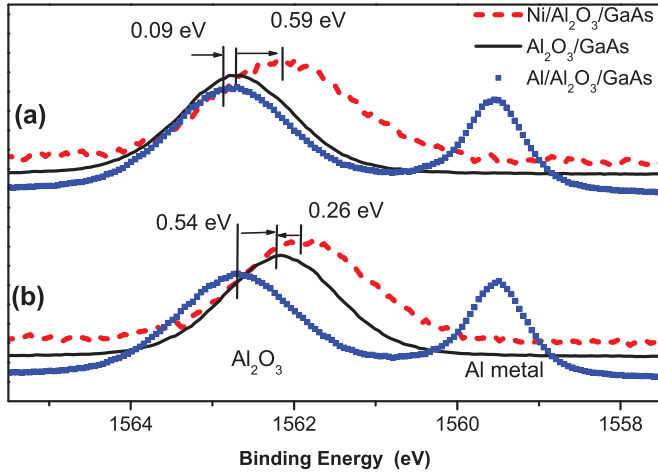


FIG. 7. (Color online) Al 1s spectra showing BE shift due to the changes in the potential across the Al_2O_3 layer caused by different work-function metals for (a) *n*-type and (b) *p*-type GaAs. The presence of a metallic Al 1s signal at 1559.5 eV binding energy originates from the metal cap.

type, of 0.11–0.31 eV, and *p* type, of 0.15–0.35 eV as shown in Table I.

Work-function differences between the metal and the pinned GaAs Fermi level should be reflected in a potential difference across the dielectric layer resulting in a binding energy shift, and broadening of the associated dielectric core levels.³ These changes would be expected to be most apparent between the *n*-type GaAs and the Ni, or the *p*-type GaAs and the Al, as these both represent the largest potential difference, given the electron affinity of GaAs is 4.07 eV. Figure 7 shows the changes in binding energy of the Al 1s oxide peak (located at 1562 eV) for the *n*- and *p*-type GaAs substrate resulting from metal deposition. For the *n*-type sample the deposition of the low work-function Al results in a small increase in the Al 1s peak BE (0.09 eV), which is less than the work-function difference in the range of 0.3–0.5 eV. It is thought that this discrepancy is partly due to trapped charge in the Al_2O_3 , which has previously been measured in the case of $\text{Al}_2\text{O}_3/\text{InGaAs}$ systems.^{28,29} If there is positive charge already present in the oxide then the potential field needed to equalize the metal work-function and Fermi level in the semiconductor is less in the case of an Al cap, and greater in the case of an Ni cap, which is the case in our results as shown in Table II. The presence of a metallic Al 1s signal at 1559.4 eV binding energy originates from the gate metal. For the Ni capped *n*-type sample, a

significant decrease in the binding energy (−0.59 eV) of the Al 1s oxide peak reflects a potential difference of the opposite polarity across the dielectric caused by the high work-function Ni contact, as previously explained by Walsh *et al.*⁵ and this shift agrees well with the theoretical work-function difference in the range from −0.52 to −0.32 eV. The corresponding binding energy shifts for the *p*-type sample were 0.54 eV to higher BE with the Al cap and −0.26 eV for the Ni cap, which agree well with the expected shifts of 0.66–0.86 eV and −0.12 to 0.08 eV, respectively.

All of these changes are consistent with the difference in the polarity of the potential difference in the dielectric layer caused by the low and high work-function metals and further reflect the restricted nature of the Fermi level movement in the GaAs, as the work-function difference between GaAs and metal caps is manifest as a potential difference across the dielectric layer.³ The Al 1s peak widths for the metal capped samples broaden when compared to the samples without metal gates reflecting the gradient in the potential across the dielectric layer. The small potential difference of 0.09 eV measured across the Al_2O_3 layer for the Al on *n* type results in negligible broadening while a full width half maximum (FWHM) increase of 0.36 eV for Ni on the *n*-type reflects the larger potential difference across the dielectric. In the case of the *p*-type sample, again negligible differences in FWHM were measured for the Al contact, but a 0.18-eV FWHM increase was found for the Ni capped sample. While these differences are smaller than would be expected, this can be partially accounted for by the limited extent to which these potential changes can be quantified by measuring photoemission peak line shapes.³⁰

IV. CONCLUSIONS

In summary, the large sampling depth of HAXPES has been used to characterize band bending in metal/ Al_2O_3 /GaAs (MOS) structures fabricated with both high (Ni) and low (Al) work-function metals. The results are consistent with different Fermi level positions for *n*- and *p*-doped substrates which are largely independent of metal work function. Valence band measurements indicate that the Fermi level positions in the band gap are in the range of 0.4–0.75 eV and 0.8–1.11 eV above the valence band maximum for *p*-type and *n*-type GaAs, respectively. C-V analysis of near identical samples yield very similar surface Fermi level positions at zero gate voltage for the *n*- and *p*-type GaAs samples. The C-V responses also indicate an Al_2O_3 /GaAs interface with a higher D_{it} in the upper half of the band gap. A potential difference across the Al_2O_3 layer consistent with the difference in metal work functions was also measured. The ability of HAXPES measurements to allow the extraction of Fermi level positions at buried metal/dielectric interfaces in the presence of metal capping layers facilitates the study of MOS structures which are difficult to analyze by C-V electrical characterization methods due to the limited Fermi level movement. The fact that HAXPES measurements can also provide information on chemical interactions makes it a powerful analytical tool for the investigation of MOS structures with layer thickness dimensions relevant to future semiconductor device technology nodes.

TABLE II. Comparison of the calculated and measured shifts in the Al oxide peak due to the presence of a potential field across the oxide layer.

Sample	Calculated Al_2O_3 shift (eV)	Experimental Al_2O_3 shift (eV)
Al/ Al_2O_3 / <i>n</i> -GaAs	0.3 – 0.5	0.09
Ni/ Al_2O_3 / <i>n</i> -GaAs	−0.52 – −0.32	−0.59
Al/ Al_2O_3 / <i>p</i> -GaAs	0.66 – 0.86	0.54
Ni/ Al_2O_3 / <i>p</i> -GaAs	−0.12 – 0.08	−0.26

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- ¹K. Kobayashi, M. Yabashi, Y. Takata, T. Tokushima, S. Shin, K. Tamasaku, D. Miwa, T. Ishikawa, H. Nohira, T. Hattori, Y. Sugita, O. Nakatsuka, A. Sakai, and S. Zaima, *Appl. Phys. Lett.* **83**, 1005 (2003).
- ²P. S. Lysaght, J. Barnett, G. I. Bersuker, J. C. Woicik, D. A. Fischer, B. Foran, H.-H. Tseng, and R. Jammy, *J. Appl. Phys.* **101**, 024105 (2007).
- ³K. Kakushima, K. Okamoto, K. Tachi, J. Song, S. Sato, T. Kawanago, K. Tsutsui, N. Sugii, P. Ahmet, T. Hattori, and H. Iwai, *J. Appl. Phys.* **104**, 104908 (2008).
- ⁴R. Claessen, M. Sing, M. Paul, G. Berner, A. Wetscherek, A. Müller, and W. Drube, *New J. Phys.* **11**, 125007 (2009).
- ⁵L. A. Walsh, G. Hughes, P. K. Hurley, J. Lin, and J. C. Woicik, *Appl. Phys. Lett.* **101**, 241602 (2012).
- ⁶G. Brammertz, H. C. Lin, K. Martens, D. Mercier, C. Merckling, J. Penaud, C. Adelmann, S. Sioncke, W. E. Wang, M. Caymax, M. Meuris, and M. Heyns, *J. Electrochem. Soc.* **155**, H945 (2008).
- ⁷C. C. Fulton, G. Lucovsky, and R. J. Nemanich, *J. Appl. Phys.* **99**, 063708 (2006).
- ⁸D. Mao, A. Kahn, G. Le Lay, M. Marsi, Y. Hwu, and G. Margaritondo, *Appl. Surf. Sci.* **56-58**, Part 1, 142 (1992).
- ⁹M. Caymax, G. Brammertz, A. Delabie, S. Sioncke, D. Lin, M. Scarrozza, G. Pourtois, W.-E. Wang, M. Meuris, and M. Heyns, *Microelectron. Eng.* **86**, 1529 (2009).
- ¹⁰I. Lindau, T. Kendelewicz, N. Newman, R. List, M. Williams, and W. Spicer, *Surf. Sci.* **162**, 591 (1985).
- ¹¹R. Engel-Herbert, Y. Hwang, and S. Stemmer, *J. Appl. Phys.* **108**, 124101 (2010).
- ¹²E. O'Connor, B. Brennan, V. Djara, K. Cherkaoui, S. Monaghan, S. B. Newcomb, R. Contreras, M. Milojevic, G. Hughes, M. E. Pemble, R. M. Wallace, and P. K. Hurley, *J. Appl. Phys.* **109**, 024101 (2011).
- ¹³S. Tanuma, C. J. Powell, and D. R. Penn, *Surf. Interface Anal.* **43**, 689 (2011).
- ¹⁴J. Chastain and J. F. Moulder, *Handbook of X-ray Photoelectron Spectroscopy: A Reference Book of Standard Spectra for Identification and Interpretation of XPS Data* (Physical Electronics, Eden Prairie, 1995).
- ¹⁵E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology* (Wiley, New York, 1982).
- ¹⁶D. R. Lide, *Handbook of Chemistry and Physics: 2004-2005* (CRC Press, Boca Raton, 2004).
- ¹⁷L. Lin and J. Robertson, *Appl. Phys. Lett.* **98**, 082903 (2011).
- ¹⁸W. Wang, C. Hinkle, E. Vogel, K. Cho, and R. Wallace, *Microelectron. Eng.* **88**, 1061 (2011).
- ¹⁹E. A. Kraut, R. W. Grant, J. R. Waldrop, and S. P. Kowalczyk, *Phys. Rev. Lett.* **44**, 1620 (1980).
- ²⁰A. K. Rumaiz, J. C. Woicik, G. A. Carini, D. P. Siddons, E. Cockayne, E. Huey, P. S. Lysaght, D. A. Fischer, and V. Genova, *Appl. Phys. Lett.* **97**, 242108 (2010).
- ²¹M. Alonso, R. Cimino, and K. Horn, *Phys. Rev. Lett.* **64**, 1947 (1990).
- ²²A. Bauer, M. Prietsch, S. Molodtsov, C. Laubschat, and G. Kaindl, *J. Vac. Sci. Technol. B* **9**, 2108 (1991).
- ²³D. Yan, F. H. Pollak, T. P. Chin, and J. M. Woodall, *Phys. Rev. B* **52**, 4674 (1995).
- ²⁴T. Kendelewicz, P. Soukiassian, M. H. Bakshi, Z. Hurych, I. Lindau, and W. E. Spicer, *Phys. Rev. B* **38**, 7568 (1988).
- ²⁵W. E. Spicer, I. Lindau, P. Skeath, and C. Y. Su, *J. Vac. Sci. Technol.* **17**, 1019 (1980).
- ²⁶P. K. Hurley, E. O'Connor, S. Monaghan, R. Long, A. O'Mahony, I. M. Povey, K. Cherkaoui, J. MacHale, A. Quinn, G. Brammertz, M. M. Heyns, S. Newcomb, V. V. Afanas'ev, A. Sonnet, R. Galatage, N. Jivani, E. Vogel, R. M. Wallace, and M. Pemble, *ECS Transactions* **25**, 113 (2009).
- ²⁷N. P. Khuchua, L. V. Khvedelidze, M. G. Tigishvili, N. B. Gorev, E. N. Privalov, and I. F. Kodzhespirova, *Russian Microelectronics* **32**, 257 (2003).
- ²⁸B. Shin, J. R. Weber, R. D. Long, P. K. Hurley, C. G. Van de Walle, and P. C. McIntyre, *Appl. Phys. Lett.* **96**, 152908 (2010).
- ²⁹R. D. Long, B. Shin, S. Monaghan, K. Cherkaoui, J. Cagnon, S. Stemmer, P. C. McIntyre, and P. K. Hurley, *J. Electrochem. Soc.* **158**, G103 (2011).
- ³⁰G. Margaritondo, F. Gozzo, and C. Coluzza, *Phys. Rev. B* **47**, 9907 (1993).